7812-488

INTERFACE

KAY

INSTRUCTION MANUAL

7812-488

INTERFACE

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7812 Revisions

The 7812 has undergone substantial changes in the way that the DATA TALK mode operates. The MEMORY TALK and LISTEN modes are pretty much unchanged from the original manual description, but DATA TALK needs new explanation.

The primary change is instead of DATA TALK being a continuous flow of data that the user must somehow handle at high sample rates, now the user captures one line of data at a time, each line being a specific point on the frequency axis, until an entire Sonagram has been transferred.

The number of lines depends on the front panel FREQUENCY setting 512, 256, or 128 lines of data.

The number of points in a line is set by the TIME buttons on the front panel;4096, 2048, or 1024.bytes.) Previously, if the user had the front panel set for 4096 points and 512 lines, a buffer 2.1 megabytes long would have been necessary.

The TALK ADDRESS sequence is the same as in the manual, except that the controller only reads the selected number of points in a line, processses them, and then reads another line, until the selected number of lines has been read. The controller should send a TALK ADDRESS sequence before each line, since the 7812 uses that to re-initialize its internal counters and reset the 7800 memory to the start. DO NOT however send a UNTALK command until all the desired data has been transferred, since this would start data transfer at the beginning of the frequency axis, not at the last line read.

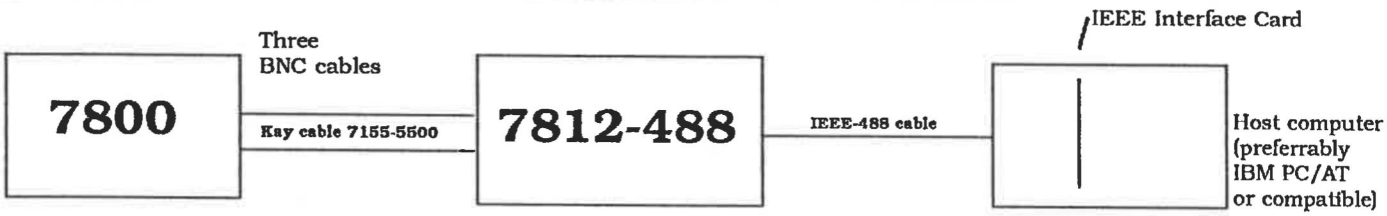
Once all the desired data is transferred, send a UNTALK command to turn off the 7812.

DIGITAL INTERFACE - OPTION 7812

Introduction

The 7812 is an option unit which must be purchased with the 7800. The 7812-488 is a separate unit which allows the Digital Sona-Graph model 7800 to connect to computers using the IEEE-488 interface. To operate the user requires a 7800, a 7812-488, connecting the 7800 to the 7812, a host computer, a IEEE-488 interface card for the host computer, a IEEE-488 cable to connect the 7812-488 to the IEEE-488 interface and software for the user's computer. Kay provides a test software program for IBM-PC compatible computers. The hardware configuration is indicated in the figure below.

Hardware Configuration

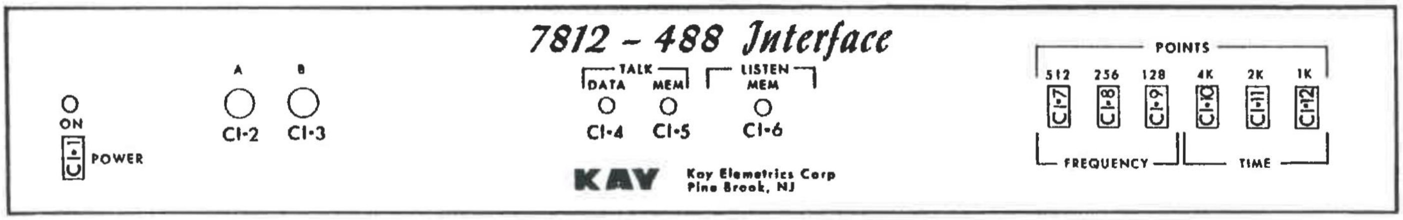


The 7812 is an instrument which acts as an interface between a host computer (controller) and the 7800. The interface is implemented by using the GPIB IEEE standard 488-1979 . There are numerous books and articles describing this bus and most computers have a GPIB Model (sometimes this is standard and sometimes the user will need to pay extra - consult your computer manufacturer). While small mirocomputers can be used as controllers their small memory makes them unsuitable for meaningful work. Kay used the GPIB, or IEEE-488 standard, due to its standardization and wide use. The 7812 instrument is sometimes referred to as the 7812-488 in this text.

Kay has provided a test software package for the IBM-PC. To work with other computers or perform different tasks, the user will need to write software on the host computer to talk and listen to the 7800 memory and to selectively display, manipulate, extract features and process the digitized graphic data. The graphic output is configured like the spectrographic display. Because the spectrographic analysis has so much information (up to 512 lines X 4096 points X 5 bits or 2 megabytes) the user will most likely not store this entire output. A graphic enhancer for many terminals may be needed to display the grey scale information (sonagram format). See the section titled 7812/7800 test software for more information

The IEEE Standard 488-1978 bus, also called the GPIB, is a bit-parallel byte-serial interface system developed to allow the transfer of digital data among a group of 15 or less disparate devices. The 488 standard insures that such things as data rate, bus configuration, impedances and asyncronous clocks present no obstruction to the interchange of data between these devices. The total transmission length of the interconnecting cables is limited to 20 meters and the maximum data rate for any signal line is 1Mb/s. However, the interconnecting cables should always be kept as short as possible. The cable used to connect the 7812-488 to the 7800 is included with the 7812-488 (Kay part # 7155-5500). The cable used to connect the 7812-488 to the GPIB should follow the specifications in the IEEE-488 standards book.

A complete description of the IEEE Std. 488-1978 Bus is available from the Instititute of Electrical Electronics Engineers, Inc, 345 East 47th Street, New York, New


7812 – 488 Interface
ON
CI-1
POWER
A
B
CI-2
CI-3
TALK
DATA
MEM
LISTEN
MEM
CI-4
CI-5
CI-6
KAY
Kay Elemetrics Corp
Pine Brook, NJ
POINTS
512
256
128
4K
2K
1K
CI-7
CI-8
CI-9
CI-10
CI-11
CI-12
FREQUENCY
TIME

York 10017. The title of the publication is "IEEE Standard Digital Interface for Programmmable Instrumentation."

Instruments on the GPIB will have one or more of the following capabilities. The ability to act as a listener, a talker, a talker-listener or as a controller. Generally there is only one system controller which may also be a talker and/or listener.

The 7812-488 instrument manufactured by Kay Elemetrics Corp interfaces three functions of the Digital Sona-Graph, model 7800 with the GPIB. The 7812-488 has two talk modes and one listen mode. The 7812-488 never acts as the controller.

The 7812-488 GPIB protocol is accomplished by a 96LS488 integrated circuit manufactured by Fairchild Camera and Instrument Corporation. A data sheet of the 96LS488 has been included in the 7812-488 manual.The data sheet describes in full all timing sequences and protocol performed by the 96LS488.

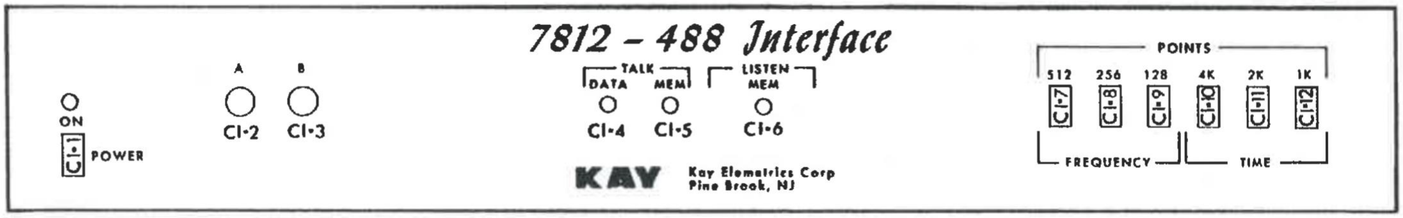
The 7812-488 incorporates two of these integrated circuits only one of which will be active at a time. The section of the 96LS488 data sheet labled 488 Bus Signals should be fully read and understood before attempting to use the 7812-488 instrument. All of the 96LS488 data that refers to the instrument side of the device can be ignored. However a knowledge of these operations can be helpful in understanding the operation of the 7812-488. The operator of the 7812-488 will have to understand the timing sequences for a Listen Address Sequence and a Talk Address Sequence and the protocol (or handshaking) required to transfer data on the GPIB.

This information is available in the 96LS488 data sheet and in the GPIB standards book.

The 7812-488 interface instrument, as previously stated, has two talk modes and one listen mode and never acts as a controller. The three different modes are:

DATA TALK
MEMORY TALK
MEMORY LISTEN

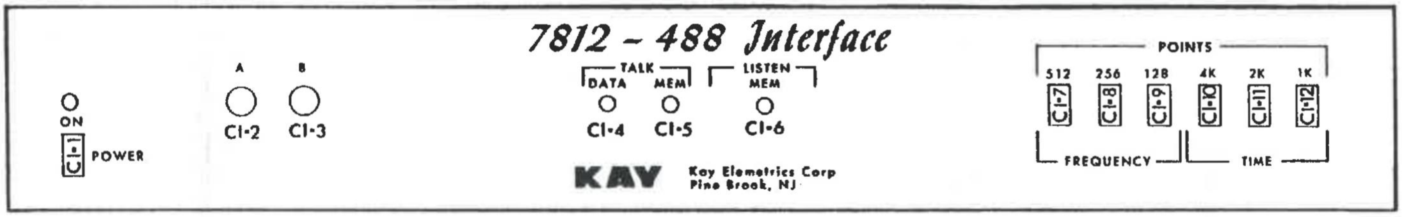
Figure #2 (on the following page) describes the instructions needed by the controller to implement the transfer of information from the 7800 to/from the host controller via the 7812.


7812 – 488 Interface
ON
CI-1
POWER
A
B
CI-2
CI-3
TALK
DATA
MEM
LISTEN
MEM
CI-4
CI-5
CI-6
KAY
Kay Elemetrics Corp
Pine Brook, NJ
POINTS
512
256
128
4K
2K
1K
CI-7
CI-8
CI-9
CI-10
CI-11
CI-12
FREQUENCY
TIME

LINE #	GPIB LEVELS								7812 MODE
	D10 8	D10 7	D10 6	D10 5	D10 4	D10 3	D10 2	D10 1	
1	*	L	H	L	H	H	H	L	DATA TALK ADDRESS
2	L	H	← DATA →						DATA TALK (6 LSB of Freq. Data)
3	H	L	← DATA →						DATA TALK (6 MSB of Freq. Data)
4	L	L	← DATA →						DATA TALK (6 Bits of Analyzed Data)
5	H	H	*	*	*	*	*	*	DATA TALK (End of Analyzed Data Transmission)
6	*	L	H	H	H	H	L	H	MEMORY TALK ADDRESS
7	*	H	L	←DATA→					MEMORY TALK (5 LSB)
8	*	L	H	←DATA→					MEMORY TALK (5 MSB)
9	*	H	L	H	H	H	L	H	MEMORY LISTEN ADDRESS
10	*	H	*	←DATA→					MEMORY LISTEN (5 LSB)
11	*	L	*	← DATA→					MEMORY LISTEN (5 MSB)
12	*	L	H	L	L	L	L	L	UNIVERSAL UNTALK
13	*	H	L	L	L	L	L	L	UNIVERSAL UNLISTEN
14									

H = High Logic Level
L = Low Logic Level
* = Doesn't Matter

Figure # 2

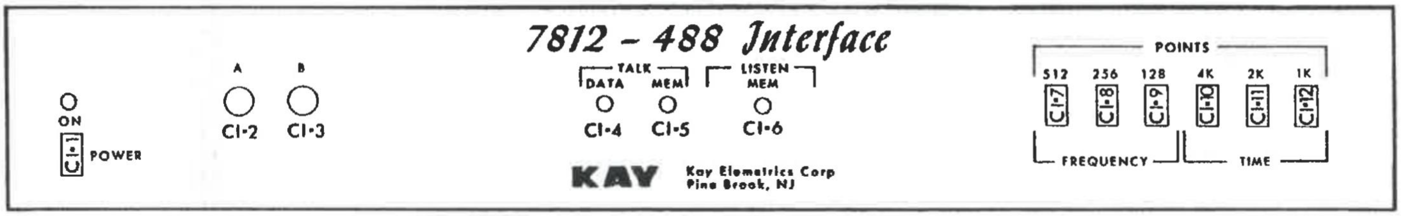

7812 – 488 Interface
ON
C1-1
POWER
A
B
C1-2
C1-3
TALK
DATA
MEM
LISTEN
MEM
C1-4
C1-5
C1-6
KAY
Kay Elemetrics Corp
Pine Brook, NJ
POINTS
512
256
128
4K
2K
1K
C1-7
C1-8
C1-9
C1-10
C1-11
C1-12
FREQUENCY
TIME

LINE #	GPIB LEVELS								7812 MODE
	D10 8	D10 7	D10 6	D10 5	D10 4	D10 3	D10 2	D10 1	
1	*	L	H	L	H	H	H	L	DATA TALK ADDRESS
2	L	H	← DATA →						DATA TALK (6 LSB of Freq. Data)
3	H	L	← DATA →						DATA TALK (6 MSB of Freq. Data)
4	L	L	← DATA →						DATA TALK (6 Bits of Analyzed Data)
5	H	H	*	*	*	*	*	*	DATA TALK (End of Analyzed Data Transmission)
6	*	L	H	H	H	H	L	H	MEMORY TALK ADDRESS
7	*	H	L	← DATA →					MEMORY TALK (5 LSB)
8	*	L	H	← DATA →					MEMORY TALK (5 MSB)
9	*	H	L	H	H	H	L	H	MEMORY LISTEN ADDRESS
10	*	H	*	← DATA →					MEMORY LISTEN (5 LSB)
11	*	L	*	← DATA →					MEMORY LISTEN (5 MSB)
12	*	L	H	L	L	L	L	L	UNIVERSAL UNTALK
13	*	H	L	L	L	L	L	L	UNIVERSAL UNLISTEN
14	128	64	32	16	8	4	2	1	

H = High Logic Level
L = Low Logic Level
* = Doesn't Matter

Figure # 2

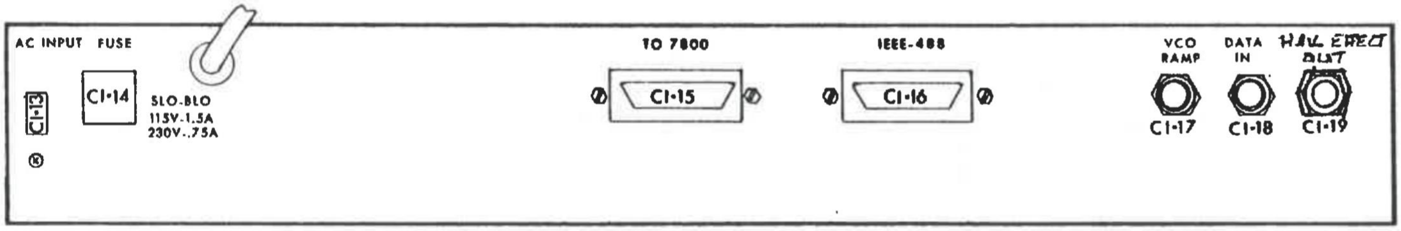
DATA TALK = 1 + 16 + 64 = 81
MEM TALK = ~~32~~ + 2 + 64 = 66
MEM LISTN = 2 + 32 = 34


7812 – 488 Interface
ON
CI-1
POWER
A
B
CI-2
CI-3
TALK
DATA
MEM
LISTEN
MEM
CI-4
CI-5
CI-6
KAY
Kay Elemetrics Corp
Pine Brook, NJ
POINTS
512
256
128
4K
2K
1K
CI-7
CI-8
CI-9
CI-10
CI-11
CI-12
FREQUENCY
TIME

Description of Panel Controls

NOTE: ***To differentiate control symbols on the Digital Sona-Graph and the optional Computer Interface, Model 7812, all controls for the Computer Interface are designated by the prefix 'CI' (i.e, CI-1 refers to control 1 on the Computer Interface model 7812).***

CONTROL SYMBOL	DESCRIPTION
CI-1	POWER ON/OFF - This switch supplies A.C. current to the power supply.
CI-2	Designed for future instrument enhancement.
CI-3	Designed for future instrument enhancement.
CI-4	DATA TALK LIGHT - This LED indicates if the 7812 is in the DATA TALK Mode. This mode allow the 7800 to output spectrographic data to the host computer through the 7812.
CI-5	MEM.TALK LIGHTS - This LED indicates if the 7812 is in the MEMORY TALK Mode. This mode allows the 7800 to output its digital memory (audio signal) directly to the host computer through the 7812.
CI-6	MEM. LISTEN LIGHT - This LED indicates if the 7812 is in the MEMORY LISTEN Mode. This mode allows the 7800 to receive digital data from the host computer and store this data directly in the 7800 digital memory for analysis.
CI-7, CI-8 CI-9	FREQUENCY POINTS (LINES) - 512, 256, 128 - These buttons control the number of frequency lines used in the DATA TALK Mode to represent a spectrogram (i.e., 128 or 256 or 512).
CI-10, CI-11, CI-12	TIME POINTS (POINTS/LINE) - 4K, 2K, 1K - These buttons control the number of points/line used in the DATA TALK Mode to represent a spectrogram (i.e, Ik or 2K or 4K).
CI-13	LINE VOLTAGE SWITCH - This switch changes the voltage from 120 to 240.
CI-14	FUSE

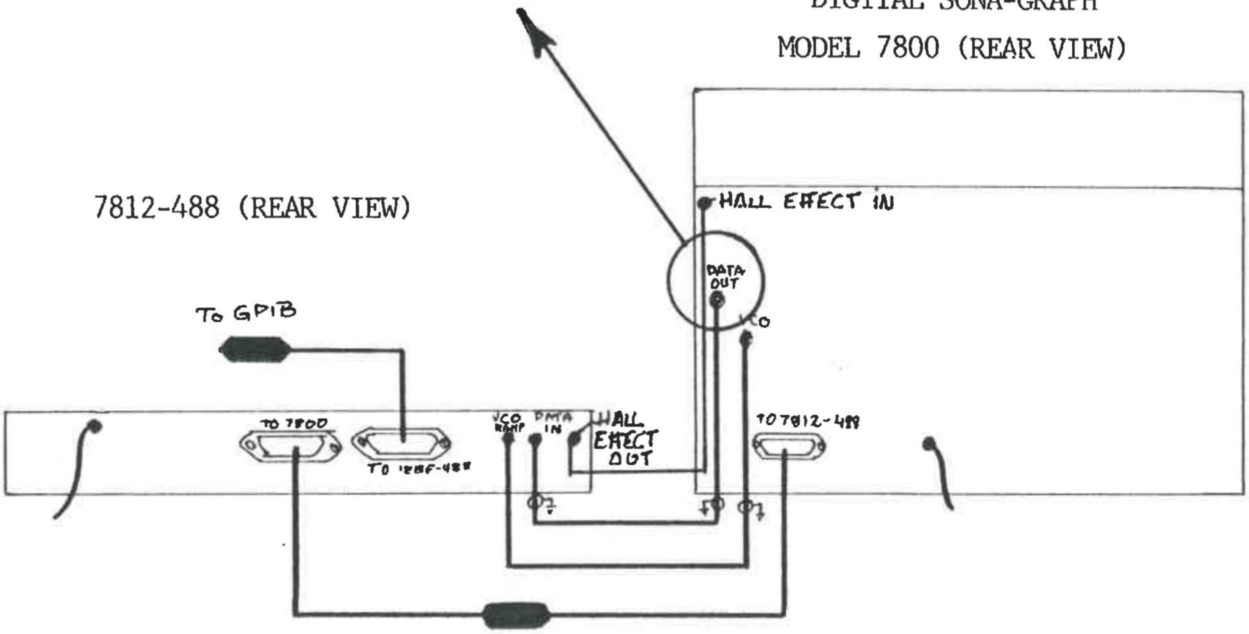

AC INPUT
FUSE
C1-13
C1-14
SLO-BLO
115V-1.5A
230V-.75A
TO 7800
C1-15
IEEE-488
C1-16
VCO
RAMP
C1-17
DATA
IN
C1-18
HALL EFFECT
OUT
C1-19

Description of Panel Controls

CONTROL SYMBOL	DESCRIPTION
CI-15	To 7800 - This connector and the included cable are used to connect the 7812 to the 7800 Digital Sona-Graph.
CI-16	TO IEEE - This connector and a customer supplied cable are used to connect the 7800/7812 combination to the IEEE.
CI-17	VCO RAMP - This BNC type connector and the supplied cable is used to connect the VCO input on the 7800 with the 7812. This connector carries the control voltage for the frequency domain from the 7812 to the 7800.
CI-18	DATA IN - This BNC type connector and supplied cable are used to connect the 7800 VERT (DATA) connector with the 7812. This connector carries the data or darkness information to the 7812.
CI-19	HALL EFFECT OUT- This BNC type connector and supplied cable are used to connect the 7800 HALL EFFECT IN with the 7812. This connector carries the triggering pulse to set the 7800 to the start of the recording.

IMPORTANT NOTICE:

The DATA OUT connector is located on the front panel of the Digital Sona-Graph.


DIGITAL SONA-GRAPH
MODEL 7800 (REAR VIEW)

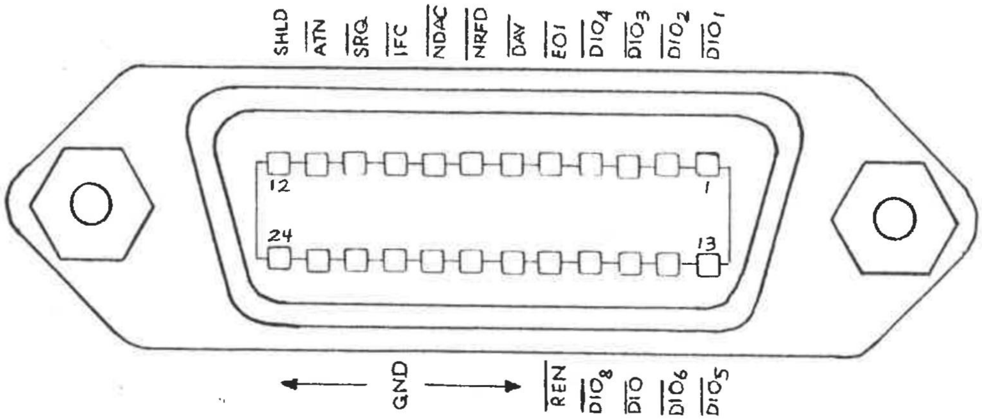
7812-488 (REAR VIEW)

HALL EFFECT IN
DATA OUT
VCO
To GPIB
TO 7800
TO IEEE-488
VCO RAMP
DATA IN
HALL EFFECT OUT
TO 7812-488

FIGURE #3

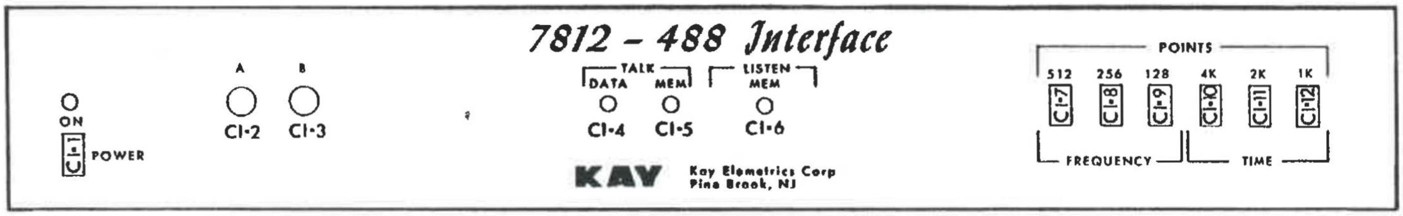
Connection of 7812 to 7800 and to GPIB

The GPIB standard specifies a connector which is a standard 24-pin industrial connector such as Cinch or Amphenol series 57 Micro-Ribbon. The cable has 16 signal lines and 8 ground lines.



There are two 24-pin connectors on the 7812-488. One is labeled TO 7800 (Control CI-15) and must be connected to a similar connector labeled TO 7812-488 (Control Z3) on the rear panel of the 7800. The other is labeled IEEE-488 and this one is connected to the GPIB. A coaxial cable must be connected to the BNC connector labeled DATA IN (Control CI-18) on the 7812-488 to the BNC connector labeled DATA on the 7800. Another coaxial cable must be connected from the BNC connector labeled VCO (Control CI-17) on the 7812-488 to the BNC connector labeled VCO IN (Control ZX2) on the rear panel of the 7800. An additional BNC Cable has been added. From 7812 "HALL EFFECT OUT" to 7800 "7812 HALL EFFECT IN".

The BNC labeled DATA OUT (Control WI) on the 7800 is the output for the analyzed spectrographic data from the 7800 to the 7812-488. The BNC labeled VCO (Control X2) on the 7800 is the input to the 7800 for the control voltage that sweeps or tunes the CARRIER OSCILLATOR in the 7800. Figure #3 shows the interconnections between the 7812-488 and the Digital Sona-Graph.


7812 – 488 Interface
ON
CI-1
POWER
A
B
CI-2
CI-3
TALK
DATA
MEM
LISTEN
MEM
CI-4
CI-5
CI-6
KAY
Kay Elemetrics Corp
Pine Brook, NJ
POINTS
512
256
128
4K
2K
1K
CI-7
CI-8
CI-9
CI-10
CI-11
CI-12
FREQUENCY
TIME

Data Talk Mode

In the DATA TALK mode, the 7812-488 will put on the GPIB the analyzed data from the ANALYSIS FILTERS and DYNAMIC RANGE circuit in the Digital Sona-Graph model 7800. Essentially, the same modulated data that is used to generate each line on a Sonagram print is placed on the GPIB. Along with this information, the frequency of the line at which the analysis is taken is also presented on the GPIB.

Generally a complete set of analyzed data from the 7800 that will appear on the GPIB will consist of 512K bytes of data, rather than the 2 megabyte maximum. This is because generally if the maximum number of points per line is required then the maximum number of lines is not required, and visa versa. Each set of analyzed data will consist of a series of data lines or strings where the CARRIER OSCILLATOR in the 7800 is held at a fixed frequency for each line of data taken.

EXAMPLE: Suppose the 7800 is in the 8kHz range and the 300Hz analysis filter is selected. For this condition the 128 LINE FREQUENCY (Control CI-9 button on the 7812-488 should be pushed in and the 4K POINTS/LINE TIME (Control CI-10) button should be pushed in. This means that a set of data will be put on the GPIB consisting of 128 lines of data with 4096 points of data along each line. Each line of data represents a new analysis at a successively higher frequency. Also, at the start of each line a set of data (2 bytes) is generated which denotes the frequency at which the data for that line was taken.

Therefore, the complete set of data generated in the example will consist of 128 lines X 4096 bytes/line + 2 bytes/line X 128 lines = 512.25K bytes (K=1024).

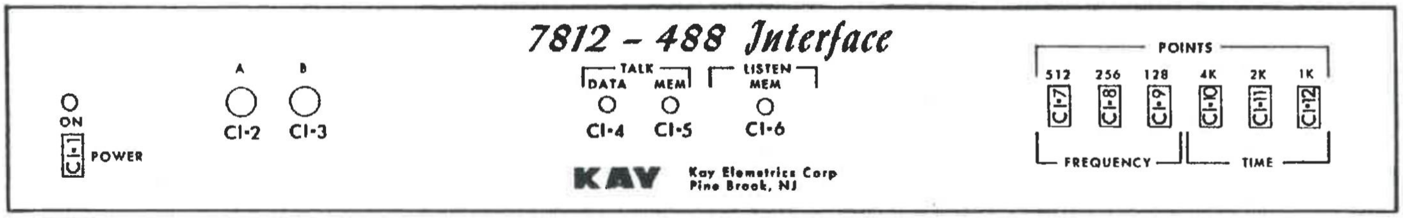
The format of the data placed on the GPIB is shown in Figure #2 on those lines labeled DATA TALK. (These are line No. 1 through 5 on the chart.

In order to activate the 7812-488 and the 7800 to operate in the DATA TALK mode the following procedure is to be used.

1. **Data to be analyzed should be recorded in the 7800 in the normal manner. Next the 7800 front panel controls should be set as if a normal Sonagram is to be made. The 7800 should be in the ANALYZE position.**

2. **The controller should first generate either an UNTALK command or issue an IFC command to assure that the 7812-488 is in a neutral state.**

3. **Next, a Primary Talk Address sequence should be issued. This sequence is shown on page 16 of the 96LS488 data sheet. The valid DATA TALK address for the 7812-488 has been set to the binary number 0111110 as shown by Figure #2 line 1. The DATA TALK address may be changed if 0111110 is inconvenient. To change the DATA TALK address remove the cover on the 7812-488 and set the DIP switch (S1) to a convenient address number. The DIP switch is marked from 1 through 10. The switches numbered 6 to 10 select the DATA TALK address. When the switches are in the ON position the GPIB signal is a HI. The DIP switch is factory set to: #6 & 10 off and #7, #8, #9, to the ON position. Switch #5 is $\overline{\text{DIO}}_5$ of the address and switch #10 is $\overline{\text{DIO}}_1$. After the controller has taken the $\overline{\text{ATN}}$ line low, the valid TALK ADDRESS should be placed on the GPIB. After about lusec, the 7812-488 will respond by taking $\overline{\text{NDAC}}$ LOW and $\overline{\text{NRFD}}$ HI. When the TALK ADDRESS is stable, the controller should take the $\overline{\text{DAV}}$ line low. Approximately lusec later, the 7812-488 takes $\overline{\text{NRFD}}$ LOW and 3 usec. later takes $\overline{\text{NDAC}}$ HI indicating the 7812-488 has**


7812 – 488 Interface
ON
C1-1
POWER
A
B
C1-2
C1-3
TALK
DATA
MEM
LISTEN
MEM
C1-4
C1-5
C1-6
KAV
Kay Elemetrics Corp
Pine Brook, NJ
POINTS
512
256
128
4K
2K
1K
C1-7
C1-8
C1-9
C1-10
C1-11
C1-12
FREQUENCY
TIME

accepted the data at this time. The TALK DATA panel indicator light should go on indicating the 7812-488 has been initialzed. The controller then takes $\overline{\mathrm{DAV}}$ high. lusec. later the 7812-488 takes $\overline{\mathrm{NDAC}}$ low and $\overline{\mathrm{NRFD}}$ hi. $\overline{\mathrm{NRFD}}$ will stay high until the controller takes $\overline{\mathrm{ATN}}$ high at which time data will begin to flow over the GBIP in accordance with the DATA TRANSFER from TALKER to GPIB protocol.

The FREQUENCY count can attain the decimal number 1600. The GPIB is an 8 bit (byte wide) BUS. An 11 bit number is needed to represent the FREQUENCY count. Figure #2 lines 2 and 3 shows the coding for the binary equivalent of the FREQUENCY count number. $\overline{\mathrm{DIO}}_8$ and $\overline{\mathrm{DIO}}_7$ are used to identify the different outputs on the GPIB for the DATA TALK mode of operation.

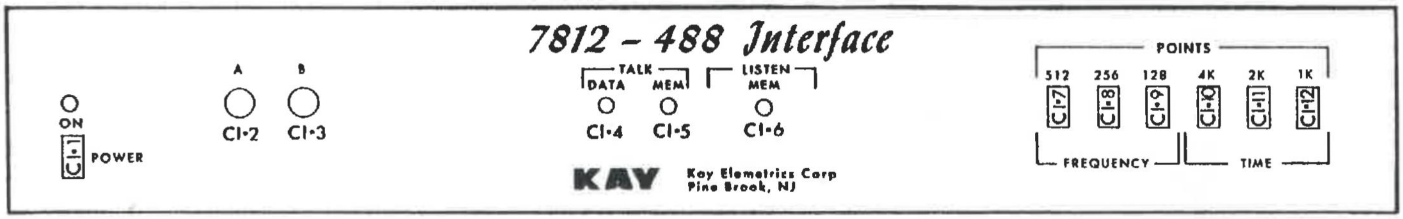
The analyzed data will appear as shown in line 4 of Figure #2. Since the information from the 7800 is compressed by the DYNAMIC RANGE settings of the 7800 the data will need less than 64 levels to allow 60dB of data variation to be transmitted on data (i.e., when the FREQUENCY count reaches the highest number for the analysis range selected on the 7800, the data transmission is interrupted and $\overline{\mathrm{DIO}}_8$ and $\overline{\mathrm{DIO}}_7$ are both high as indicated in Figure #2 on line 5). All data from the 7812-488 to the GPIB is straight binary code between 0 and 2_6 where 0 equals no energy and 2_6 equals maximum signal level.

The 7812-488 will remain in the DATA TALK mode until either an UNTALK command or an IFC command is issued. The flow of data from the 7812-488 to the GPIB must be at a rate fast enough to assure no data is missed. This rate must be consistant with the ANALYSIS FILTER chosen on the 7800. The 7812-488 offers 3 different rates which may be chosen to agree with the ANALYSIS FILTER being used on the 7800. The maximum rate is 19.2kHz which will give 4096 data points along one line of data. This rate should be used with the wide band filters on the 7800. To determine the mimimum data rate for the selected ANALYSIS FILTER use the following formula:

$$\frac{\mathbf{307.2}}{\mathbf{RANGE\ (kHz)\ OF\ 7800}} \quad \mathbf{X} \quad \mathbf{ANALYSIS\ FILTER\ (kHz)} = \mathbf{(kHz)}$$

The rate selected on the 7812-488 by the push button labeled POINTS TIME (Controls CI-10, 11, 12) must be greater than the rate number obtained by the formula. Refer to Figure #1 for what rate each button specifies.

The system computer must be able to handshake the GPIB at a rate faster than the rate being used on the front panel of the 7812-488.


7812 – 488 Interface
ON
POWER
CI•1
A
B
CI•2
CI•3
TALK
DATA
MEM
LISTEN
MEM
CI•4
CI•5
CI•6
KAY
Kay Elemetrics Corp
Pine Brook, NJ
POINTS
512
256
128
4K
2K
1K
CI•7
CI•8
CI•9
CI•10
CI•11
CI•12
FREQUENCY
TIME

Memory Listen Mode

The MEMORY LISTEN mode of operation allows an operator to input digital data to the 7800 memory. In this mode of operation, the digital storage in the 7800 is only accessible in a serial manner. That is, the memory does not act as a random access memory. If the 7812-488 is taken out of the MEMORY LISTEN mode, the memory counter in the 7800 will advance the memory location and continue to do so at a rate determined by the 7800 clock. When the 7812-488 is again initialized for the MEMORY LISTEN mode, the memory location addressed will be indeterminate.

Therefore, when a set of data is to be stored in the 7800, the whole set should be stored before the program is interrupted. If the data is insufficient to fill the 7800 memory (64K words X 10 bit) then the program should have provisions for sending data = 0 for the remainder of the memory to erase any residual signal stored in the memory.

The data can be stored in the 7800 at a 307kHz rate max. for each set of 5 bits of data (see Figure #5). At this rate the time to fill the memory is 213 msec.

To initialize the 7812-488 for the MEMORY LISTEN mode the same general sequence as the DATA TALK mode is followed except of course the address is different from the DATA TALK address. The address code for the MEMORY LISTEN is set to 1011101 and is listed in Figure #2, line #9. (The address for MEMORY LISTEN and MEMORY TALK are always the same). This address may be changed. In order to do so DIP switch S1 positions 1 through 5 select the address number. The cover of the 7812-488 must be removed in order to change the address. When the switches of S1 are in the ON position the data put on the GPIB is HI (or 1). Switch #1 of S1 is $\overline{DIO_1}$ and switch #5 is $\overline{DIO_5}$ of the GPIB lines. All address numbers allowed by the IEEE-488 standards are allowed by the 7812-488.

The Digital Sona-Graph, model 7800 memory is 64K by 10bit and the GPIB is a byte wide (8 bit) BUS. In order to use the full memory of the 7800, the data to the 7800 memory bank is split into two 5 bit sections. Information recorded in the 7800 through the 7812-488 uses bit 7 ($\overline{DIO_1}$) as a coding bit. Figure #5 shows the format for recording data into the 7800.

$\overline{D10}_8$	$\overline{D10}_7$	$\overline{D10}_6$	$\overline{D10}_5$	$\overline{D10}_4$	$\overline{D10}_3$	$\overline{D10}_2$	$\overline{D10}_1$	DATA
*	H	*	←—— DATA ——→					5 LSB of DATA
*	L	*	←—— DATA ——→					5 MSB of DATA

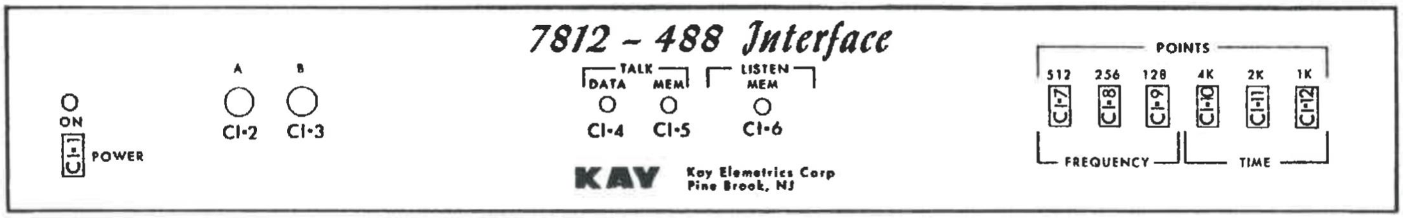
* = Doesn't matter

Figure #5

(To retrieve the data recorded see section on MEMORY TALK)

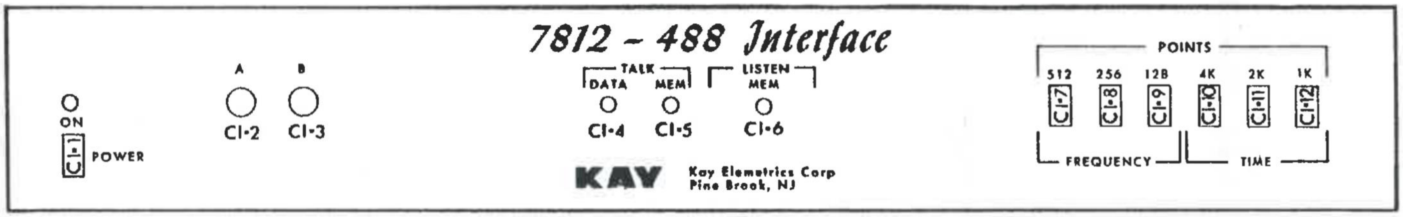
The 7800 should be in a "normal" operating mode and the ANALYZE button pushed in. There are no control settings on the 7812-488 panel for this operation. All data flow between the 7812-488, Digital Sona-Graph 7800 and the GPIB follows the IEEE 488 protocol.

After a correct LISTEN ADDRESS sequence has been done the LISTEN MEMORY light on the 7812-488 panel should be lit. The 7812-488 is now ready to receive data in the form shown in Figure #2 lines 10 & 11 and in Figure #5.


7812 – 488 Interface
ON
CI-1
POWER
A
B
CI-2
CI-3
TALK
DATA
MEM
LISTEN
MEM
CI-4
CI-5
CI-6
KAY
Kay Elemetrics Corp
Pine Brook, NJ
POINTS
512
256
128
4K
2K
1K
CI-7
CI-8
CI-9
CI-10
CI-11
CI-12
FREQUENCY
TIME

One use of the LISTEN MEMORY function would be to put in the Sona-Graph memory previously digitized speech without having to first convert the signal to analog and then redigitize it in the 7800's A/D converter.

The rate of data transferred to the 7800 in the LISTEN MEMORY mode is rate independent with a maximum transfer rate of 307kHz.


7812 – 488 Interface
ON
CI-1
POWER
A
B
CI-2
CI-3
TALK
DATA
MEM
LISTEN
MEM
CI-4
CI-5
CI-6
POINTS
512
256
128
4K
2K
1K
CI-7
CI-8
CI-9
CI-10
CI-11
CI-12
FREQUENCY
TIME
KAY
Kay Elemetrics Corp
Pine Brook, NJ

7812-488 Memory Talk Mode

The MEMORY TALK mode of operation allows an operator to retrieve the digitized data stored in the memory bank of the Digital Sona-Graph 7800. The addressing sequence of the 7812-488 for this mode of operation is similar to the DATA TALK mode except the address number is the same as the MEMORY LISTEN mode. These addressing sequences are described in the 96LS488 data sheet and in the section called DATA TALK mode.

The MEMORY TALK address may be changed but must be the same as the MEMORY LISTEN address (see section titled MEMORY LISTEN MODE). The memory in the 7800 is 64K by 10 bits and the GPIB is byte wide. Therefore, the data is taken from the 7800 as two 5 bit blocks. The $\overline{DIO_6}$ bit and the $\overline{DIO_7}$ bit are used to differentiate between the 5 LSBs and the 5 LSBs and the 5 MSBs. Figure #2 lines 6, 7, and 8 describe the factory set address and the data format of the MEMORY TALK mode.

The 7800 should be in the ANALYZE position. The maximum data rate is 307kHz and the flow of data follows the IEEE 488 protocol routine.

When the 7812-488 is addressed for the MEMORY TALK mode, the front panel indicator marked TALK MEMORY will be lit.

✓

KAY 7812/7800 Test Software

There are several requirements to run Kay's test software:

1. **You must have IBM or compatible BASIC on your machine.**

2. **You must have an IO-TECH Personal 488 Interface card.**
   (IO-TECH 23400 Aurora Road, Cleveland, Ohio 44146 (216) 439-4091

3. **An EGA card is recommended, but it will work with CGA.**

INSTRUCTIONS:

Enter into BASIC and run "7812test". The following menu will appear:

1. **Run CGA Analyze module**
2. **Run EGA Analyze module**
3. **Read 7800 memory and store on disk**
4. **Get data from disk and Write to 7800**
5. **Quit**

DATA TALK

This mode is tested by the first two options in the menu. If you have an EGA card, use (2). If not, you must use (1). The difference is that EGA mode will provide 16 levels of color while CGA will only do 4 colors.

The two options are indentical to the user in the way they execute, only the assembly subroutines which draw the screen are different. The following instruction therefore applies to both options.

The user will be first prompted to enter what TIME is selected on the 7812 front panel. Enter the number and press return.

The user then will be prompted to enter what FREQUENCY is selected. Enter the number and press return.

The program will display your selections and prompt you to verify that they are correct. Press "y" then return if so, otherwise press "n" and return to re-enter numbers.

The program will then ask you if you want to "expand" the sonagram. Expanding means drawing every point captured at the start of a line and stopping when the screen is full. Only 256 pixels are drawn in EGA mode. So that means in 2048 TIME mode, for example, only one out of every eight points is normally written to the screen. Expanding draws every point, so in 2048 TIME mode, the expansion is 8 to 1. Press return to skip past, or press "y" and return for expansion.

If everything is working, the program will switch into graphics mode and begin to draw a sonagram on the screen. Frequency information is displayed at the bottom of the screen and should correspond with the frequency counter on the 7800.

Upon completion of the sonagram, the program will prompt you to draw another sonagram. This enables the user to record new data in the 7800 and quickly display it without resetting any buttons or program variables. If you don't want to draw again, press "n" and return. The original "7812test" menu will appear on the screen.

MEMORY TALK and LISTEN

The user doesn't have to do that much to test these modes. When a recording in the 7800 is to be saved, select option (3) and the 7800 memory will be transferred into the computer in eight sections. Each section is stored on disk under the name "sonax.dta" where "x" is numbers 1 through. Each file is 16k long, adding up to 128k total of data. If the user wants to save this data, the files should be copied onto another disk or sub-directory, since the program always uses the same file names.

To write to the 7800, select option (4) and the files "sonax.dta" will be transferred back to the 7800.

When each of these operations is complete, the original "7812test" menu screen will reappear.

KAY ELEMETRICS SINGLE LEVEL BILL DATE 5/23/88
FROM-7152-2201 TO-7152-2201 OPER EDC

PARENT ITEM NO. 7152-2201
DESCRIPTION CABLE ASSY MO2 & LATER 7812
ENGR DRAW
BATCH QTY 1

LL CD	COMPONENT ITEM NO.	DESCRIPTION	ENGINEERING DRAWING NUMBER	QUANTITY	UM	ITEM TYP
04	1231-0006	HOUSING,12CKT AMP 1-640441-2		2.000	EA	4
03	1232-0005	COVER,12CKT,AMP1-640550-2		2.000	EA	4
03	1250-0200	CONN,1-551198-1,STRAIN RELIEF		2.000	EA	4
03	1250-0201	CONN,AMP 2-552273-1,24 CONT		1.000	EA	4
03	7155-6803	JACK SCREW 4-40		2.000	EA	4
03	8125-0030	CABLE, PANDUIT #100F24V12N2C		3.500	FT	4

PARENT ITEM NO. 7155-3193
DESCRIPTION PCB WIRED-BUFFER BD 7812
ENGR DRAW
BATCH QTY 1

LL CD	COMPONENT ITEM NO.	DESCRIPTION	ENGINEERING DRAWING NUMBER	QUANTITY	UM	ITEM TYP
07	0101-0001	CAP, .001MFDX100V,5%,NIC NEM		1.000	EA	4
08	0101-0013	CAP, .1MFDX100V,5%,NIC NEM		1.000	EA	4
06	0141-0029	CAP,500PF,ELMENCO #DM15-501		3.000	EA	4
08	0181-0013	CAP, 10MFDX35V,CAPAR #CLE-L		3.000	EA	4
07	0201-0124	IC, SN74LS244N, TI		2.000	EA	4
06	0201-0127	IC, DM74LS08N, NSC		1.000	EA	4
07	0201-0183	IC, 74LS157N, SIG		4.000	EA	4
06	0201-0188	IC, DM74LS123N, NSC		1.000	EA	4
05	0490-0019	RELAY,AROMAT HA1-DC12V		1.000	EA	4
06	0683-0014	RES, 332 OHM. CR25		1.000	EA	4
06	0683-0015	RES, 475 OHM, CR25		1.000	EA	4
08	0683-0024	RES, 10K OHM, CR25		4.000	EA	4
06	0683-0034	RES, 392 OHM, CR25		1.000	EA	4
08	0683-0036	RES, 681 OHM, CR25		3.000	EA	4
05	0683-0038	RES, 1500 OHM, CR25		1.000	EA	4
08	1210-0052	SOCKET,14PIN,AMP #2-641-609-3		1.000	EA	4
08	1210-0053	SOCKET,16-PIN,AMP 2-641610-3		5.000	EA	4
07	1210-0055	SOCKET,20 PIN,PCI #LSO-320-T		2.000	EA	4
08	1230-0001	HEADER,4CKT, AMP 640456-4		1.000	EA	4
08	1230-0002	HEADER, 7CKT, AMP 640456-7		1.000	EA	4
06	1230-0003	HEADER, 10 CKT, AMP 1-640454-0		2.000	EA	4
06	1230-0004	HEADER,15CKT, AMP 1-640454-5		1.000	EA	4
08	1230-0016	HEADER,12CKT,AMP 1-640454-2		3.000	EA	4
06	1854-0008	TRANS, 2N3566 FSC NPN-SI		2.000	EA	4
08	1901-0015	DIODE, 1N4446, FSC		1.000	EA	4
03	7155-3103	PCB BUFFER 7812		1.000	EA	4

PARENT ITEM NO. 7155-3500
DESCRIPTION 7812 COMPUTER INTERFACE
ENGR DRAW
BATCH QTY 1

LL CD	COMPONENT ITEM NO.	DESCRIPTION	ENGINEERING DRAWING NUMBER	QUANTITY	UM	ITEM TYP
01	5178-1299	IEEE STANDARD 488-1978/IEEE		1.000	EA	4
01	7153-5502	CABLE, PASTERNACK #PE3067-48		2.000	EA	4
01	7155-35LK	LOCK UP		1.000	EA	9
01	7155-35TC	TEST		1.000	EA	9
01	7155-5500	CABLE ASSY 7812		1.000	EA	2
01	7155-5600	ELECTRICAL ASSY 7812		1.000	EA	1
01	7155-6300	COVER 7812		1.000	EA	2
01	7155-6500	BUFFER ASSY 7812		1.000	EA	1

PARENT ITEM NO. 7155-5493
DESCRIPTION PCB WIRED,F/P 7812
ENGR DRAW
BATCH QTY 1

LL CD	COMPONENT ITEM NO.	DESCRIPTION	ENGINEERING DRAWING NUMBER	QUANTITY	UM	ITEM TYP
06	1230-0003	HEADER, 10 CKT, AMP 1-640454-0		1.000	EA	4
05	3104-0018	SWITCH,CRL,3-STA,INT,2P PB15 B14921		2.000	EA	4
04	7155-5403	PCB KAY 7812		1.000	EA	4

KAY ELEMETRICS SINGLE LEVEL BILL DATE 5/23/88
FROM-7155-5493 TO-7155-5800
OPER EDC

PARENT ITEM NO. DESCRIPTION CABLE ASSY 7812 BATCH QTY 1
7155-5500 ENGR DRAW

LL CD	COMPONENT ITEM NO.	DESCRIPTION	ENGINEERING DRAWING NUMBER	QUANTITY	UM	ITEM TYP
02	1250-0242	CONN,AMP 2-552076-1.COVER 24-P		2.000	EA	4
02	1250-0244	CONN,AMP 552283-1,PLUG 24 POS		2.000	EA	4
02	7155-6801	SCREW 4-40, DWG #A15568		2.000	EA	2
02	7155-6804	SCREW 4-40		2.000	EA	4
02	7156-4401	MARKER,		1.000	EA	2
02	7156-4402	MARKER		1.000	EA	2
03	8125-0030	CABLE, PANDUIT #100F24V12N2C		6.000	FT	4

PARENT ITEM NO. DESCRIPTION ELECTRICAL ASSY 7812 BATCH QTY 1
7155-5600 ENGR DRAW

LL CD	COMPONENT ITEM NO.	DESCRIPTION	ENGINEERING DRAWING NUMBER	QUANTITY	UM	ITEM TYP
02	7155-2500	FRAME ASSY 7812	D15525	1.000	EA	1
02	7155-5700	CHASSIS ASSY 7812		1.000	EA	1
02	7155-5800	FRONT PANEL ASSY 7812		1.000	EA	1

PARENT ITEM NO. DESCRIPTION CHASSIS ASSY 7812 BATCH QTY 1
7155-5700 ENGR DRAW

LL CD	COMPONENT ITEM NO.	DESCRIPTION	ENGINEERING DRAWING NUMBER	QUANTITY	UM	ITEM TYP
03	0360-0001	TERMINAL STRIP, CINCH #51-F		1.000	EA	4
04	0562-0024	BUMPER FEET,HH SMITH 2183		4.000	EA	4
07	0683-0011	RES, 150 OHM, CR25		1.000	EA	4
05	1111-0310	SLEEVE,FERRULE,AMP #325013		2.000	EA	4
03	1111-0365	PRW SUPPLY,CONDOR TAA-16W		1.000	EA	4
05	1111-0367	PLUG,7/16"BLK,PLAS & MET#DP437		1.000	EA	4
06	1231-0001	HOUSING,4CKT,AMP 640441-4		1.000	EA	4
08	1231-0002	HOUSING,7CKT,AMP 640441-7		2.000	EA	4
08	1231-0003	HOUSING,10 CKT.AMP 1-640441-0		2.000	EA	4
06	1232-0001	COVER, 4CKT,AMP 640550-4		1.000	EA	4
07	1232-0002	COVER,7CKT,AMP 640550-7		2.000	EA	4
05	1232-0003	COVER,10CKT,AMP 1-640550-0		2.000	EA	4
05	1250-0008	CONN, UG625B/U, BNC RECEPT		2.000	EA	4
05	1250-0193	CONN,AMP 2-323934-2, FERRULE		2.000	EA	4
03	1250-0239	CONN,AMP 552633-4,JACKSCRW SET		1.000	EA	4
04	1252-0006	STRAIN RELIEF, HEYMAN SR5-P4		1.000	EA	4
04	1400-0003	FUSEHOLDER,LITTLEFUSE 348811		1.000	EA	4
04	1400-0004	CAP,HOLDER,RED,LITLFUSE 348001		1.000	EA	4
05	2110-0016	FUSE, 1-1/2 AMP, SLO-BLO		1.000	EA	4
03	2200-0139	SCREW, 6-32 X 1/4" NYLON RHMS		4.000	EA	4
04	3101-0028	SWITCH,SWITCHCRAFT#46256LFRHU		1.000	EA	4
03	7135-0600	SPACER, KEYSTONE #1638		4.000	EA	4
05	7138-3909	SPACER, AMATON #8222-A-0440-0		11.000	EA	4
03	7153-2193	PCB WIRED 7812		1.000	EA	1
03	7155-2903	BRACKET, LINE CORD 7812		1.000	EA	2
03	7155-6802	JACK SCREW AMP (1250-0240)		2.000	EA	4
03	7159-6700	POWER SUPPLY SHIELD 6095		1.000	EA	2
03	7162-1600	MTG PLATE 7812, 7813, 7815		1.000	EA	9
04	8120-0002	LINE CORD,BELDEN #17237B 6FT		1.000	EA	4
03	8125-0027	CABLE,BELDEN #9534 (4 COND/SH)		1.500	FT	4

PARENT ITEM NO. DESCRIPTION FRONT PANEL ASSY 7812 BATCH QTY 1
7155-5800 ENGR DRAW

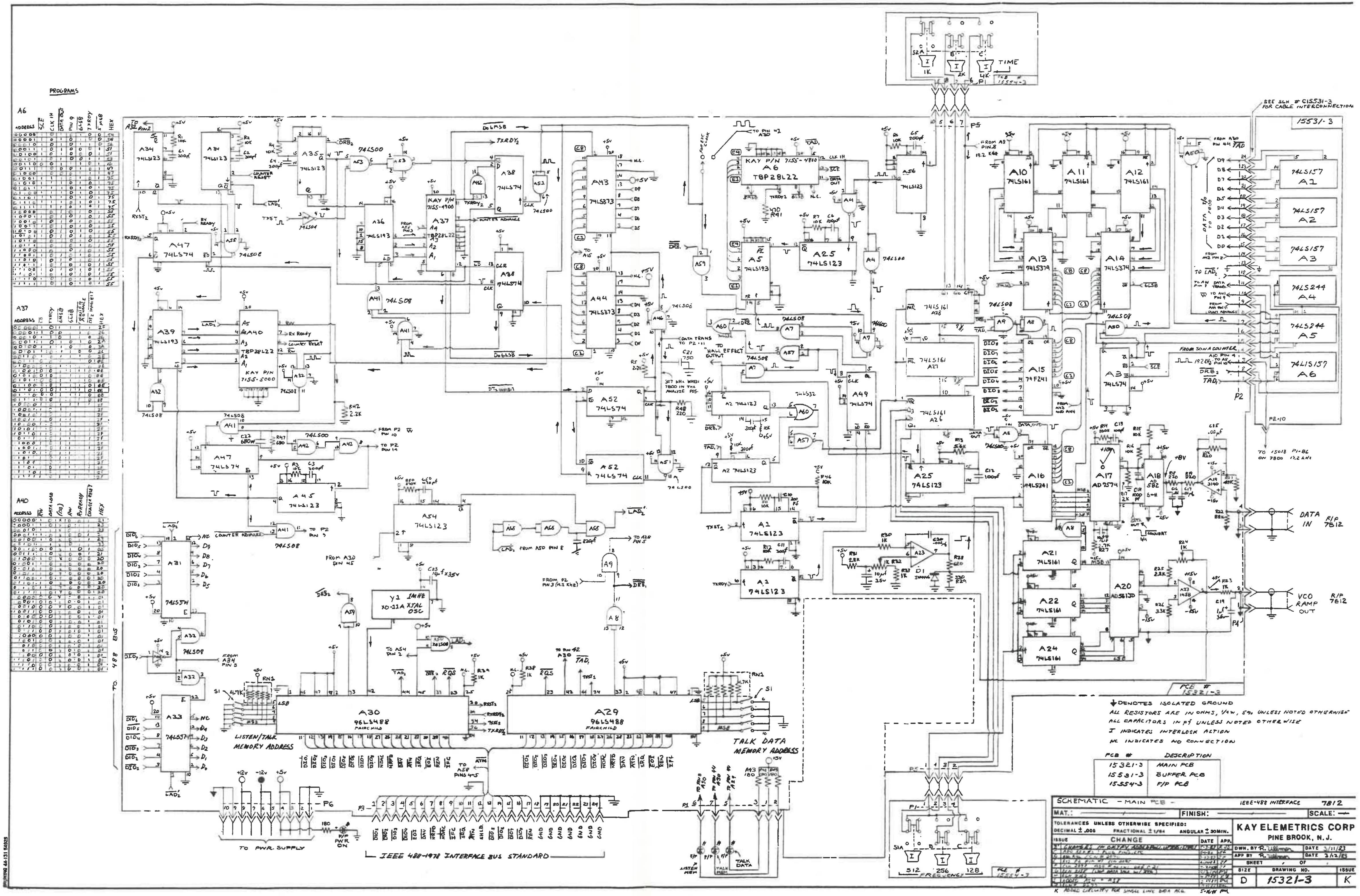
LL CD	COMPONENT ITEM NO.	DESCRIPTION	ENGINEERING DRAWING NUMBER	QUANTITY	UM	ITEM TYP
03	0372-0001	BUTTON, GRAY, B309-GY CRL		6.000	EA	4
03	1450-0039	LAMP,LED,RED,LEDCO #4000-2001		3.000	EA	4
03	3104-0039	SWITCH,COMP#881K21810T02A02		1.000	EA	4
03	7155-2803	PANEL, PAINTED + SCREENED 7812		1.000	EA	4
03	7155-5493	PCB WIRED,F/P 7812		1.000	EA	1
03	7155-6100	BKT PANEL MTG 7812		2.000	EA	2
03	7155-6200	BRACKET PCB MTG 7812		2.000	EA	2
04	7162-2201	CONN MOD (1250-0266)		1.000	EA	2

```
 KAY ELEMETRICS                       SINGLE LEVEL BILL                                  DATE  5/23/88
                               FROM-7155-6500        TO-7155-6500                         OPER EDC

PARENT ITEM NO:                 DESCRIPTION BUFFER ASSY                7812               BATCH QTY    1
7155-6500                       ENGR DRAW

         LL       COMPONENT                                            ENGINEERING                       ITEM
         CD       ITEM NO.        DESCRIPTION                          DRAWING NUMBER      QUANTITY   UM TYP

         06       1230-0003       HEADER, 10 CKT, AMP 1-640454-0                              3.000   EA  4
         08       1230-0016       HEADER,12CKT,AMP 1-640454-2                                 1.000   EA  4
         06       1231-0001       HOUSING,4CKT,AMP 640441-4                                   1.000   EA  4
         08       1231-0002       HOUSING,7CKT,AMP 640441-7                                   1.000   EA  4
         08       1231-0003       HOUSING,10 CKT,AMP 1-640441-0                               5.000   EA  4
         05       1231-0004       HOUSING,15CKT,AMP 1-640441-5                                1.000   EA  4
         04       1231-0006       HOUSING,12CKT AMP 1-640441-2                                1.000   EA  4
         06       1232-0001       COVER, 4CKT,AMP 640550-4                                    1.000   EA  4
         07       1232-0002       COVER,7CKT,AMP 640550-7                                     1.000   EA  4
         05       1232-0003       COVER,10CKT,AMP 1-640550-0                                  5.000   EA  4
         05       1232-0004       COVER, 15CKT,AMP 1-640550-5                                 1.000   EA  4
         03       1232-0005       COVER,12CKT,AMP1-640550-2                                   1.000   EA  4
         02       7152-2201       CABLE ASSY M02 & LATER    7812                              1.000   EA  1
         02       7155-3193       PCB WIRED-BUFFER BD  7812                                   1.000   EA  1
         05       7156-3700       SPACER ASM #14030-H-A-.312-13                               2.000   EA  4
         02       8125-0032       CABLE,PANDUIT#100F24V10N2C                                  2.000   FT  4
```


PROGRAMS
A6
ADDRESS
SCE
CLK IN
DATA OUT
PIN 9
6 LSB
7 TXRDY
5 MSB
HEX
A37
A40
A34 74LS123
A35 74LS123
A36 74LS193
A37 KAY P/N 7155-4900 TBP28L22
A38 74LS74
A43 74LS373
A44 74LS373
A47 74LS74
A39 74LS193
A40 KAY P/N 7155-5000 TBP28L22
A45 74LS123
A52 74LS74
A54 74LS123
A31 74LS374
A33 74LS374
A30 96LS488 FAIRCHILD
A29 96LS488 FAIRCHILD
Y1 1MHZ XO-33A XTAL OSC
LISTEN/TALK MEMORY ADDRESS
TALK DATA MEMORY ADDRESS
TO 488 BUS
TO PWR. SUPPLY
P/P PWR ON
IEEE 488-1978 INTERFACE BUS STANDARD
KAY P/N 7155-4800 A6 TBP28L22
A5 74LS193
A25 74LS123
A56 74LS123
A1 74LS123
A10 74LS161
A11 74LS161
A12 74LS161
A13 74LS374
A14 74LS374
A15 74F241
A16 74LS241
A17 AD7574
A18 S+H
A19 3140
A20 AD561JD
A21 74LS161
A22 74LS161
A24 74LS161
A26 74LS161
A27 74LS161
A28 74LS161
A49 74LS74
A3 74LS74
74LS157 A1
74LS157 A2
74LS157 A3
74LS244 A4
74LS244 A5
74LS157 A6
SEE SCH # C15531-3 FOR CABLE INTERCONNECTION
15531-3
DATA IN 7812 R/P
VCO RAMP OUT R/P 7812
TIME
FREQUENCY
512 256 128
LISTEN MEM
TALK MEM
TALK DATA
PCB # 15554-3
PCB # 15321-3
"HALL EFFECT" OUTPUT
307 KHz WHEN 7800 IN THE ANALYZE POS.
TO 15018 P1-86 ON 7800 17.2 KHz
FROM SONA COUNTER

↓DENOTES ISOLATED GROUND

ALL RESISTORS ARE IN OHMS, 1/4W, 5% UNLESS NOTED OTHERWISE

ALL CAPACITORS IN pf UNLESS NOTED OTHERWISE

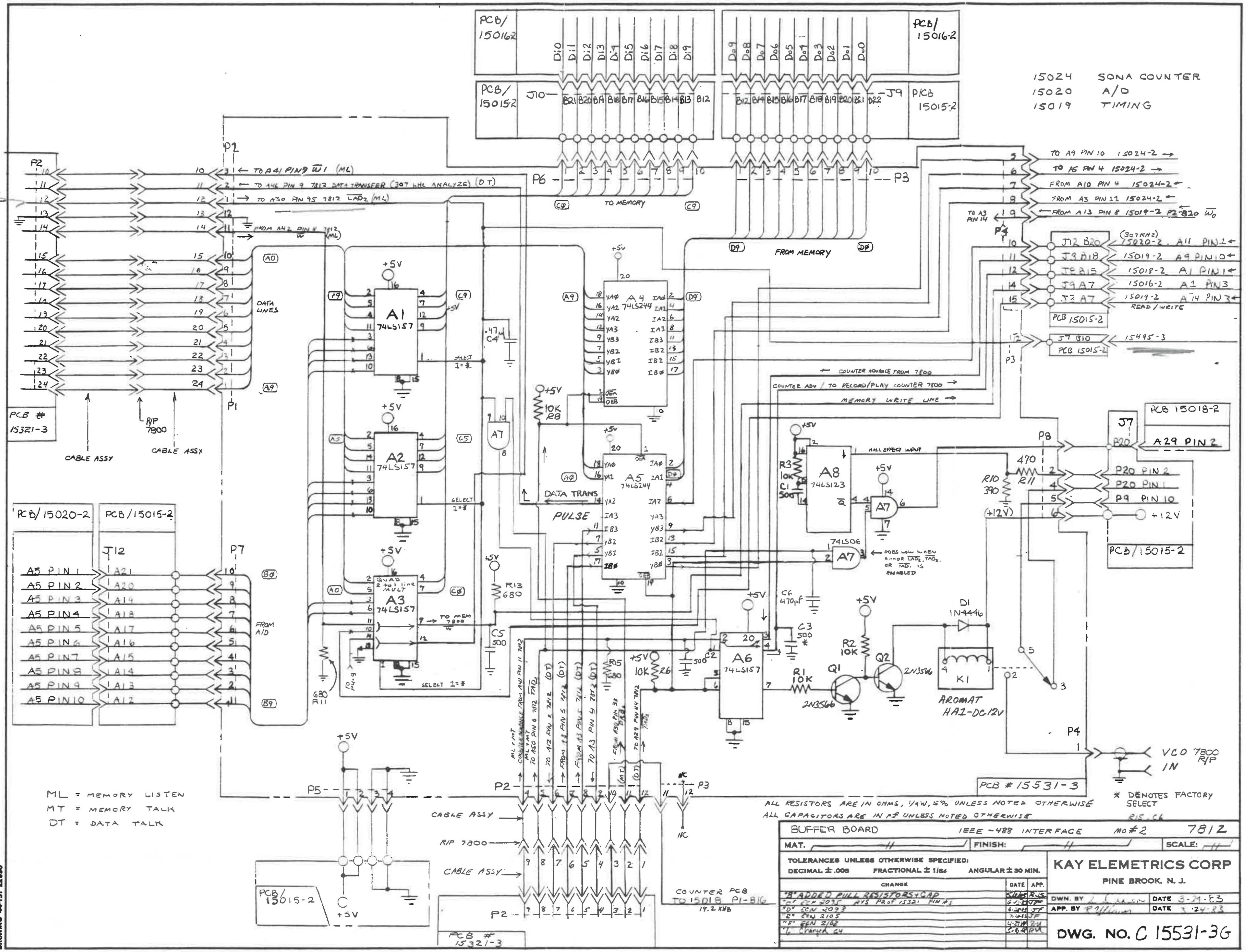
I INDICATES INTERLOCK ACTION

NC INDICATES NO CONNECTION

PCB #	DESCRIPTION
15321-3	MAIN PCB
15531-3	BUFFER PCB
15554-3	F/P PCB

SCHEMATIC - MAIN PCB -		IEEE-488 INTERFACE	7812
MAT.:		FINISH:	SCALE: —
TOLERANCES UNLESS OTHERWISE SPECIFIED: DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± 30MIN.		KAY ELEMETRICS CORP PINE BROOK, N.J.	
DWN. BY R. Ullman		DATE 3/11/83	
APP BY R. Ullman		DATE 3/12/83	
SHEET , OF			
SIZE D	DRAWING NO. 15321-3	ISSUE K	

ISSUE	CHANGE	DATE	APP.
K	ADDED CIRCUITRY FOR SINGLE LINE DATA ACQ.	5-16-8?	PM


PCB/ 15016-2
Di0 Di1 Di2 Di3 Di4 Di5 Di6 Di7 Di8 Di9
Do9 Do8 Do7 Do6 Do5 Do4 Do3 Do2 Do1 Do0
PCB/ 15015-2
J10
J9
B21 B20 B18 B16 B17 B16 B15 B14 B13 B12
B12 B14 B15 B16 B17 B18 B19 B20 B21 B22
P6
P3
TO MEMORY
FROM MEMORY
15024 SONA COUNTER
15020 A/D
15019 TIMING
P2
P1
P7
P8
P4
P5
TO A41 PIN9 W1 (ML)
TO A46 PIN 9 7812 DATA TRANSFER (307 kHz ANALYZE) (DT)
TO A30 PIN 45 7812 LAD2 (ML)
FROM A42 PIN 4 7812 W (ML)
DATA LINES
TO A9 PIN 10 15024-2
TO A5 PIN 4 15024-2
FROM A10 PIN 4 15024-2
FROM A3 PIN 11 15024-2
FROM A13 PIN 8 15019-2 P2-B20 W0
TO A3 PIN 14
J12 B20 (307 KHZ) 15020-2 A11 PIN 1
J3 B18 15019-2 A9 PIN 10
J6 B15 15018-2 A1 PIN 1
J9 A7 15016-2 A1 PIN 3
J3 A7 15019-2 A14 PIN 3
READ/WRITE
PCB 15015-2
J7 B10 15495-3
PCB 15015-2
COUNTER ADVANCE FROM 7800
COUNTER ADV / TO RECORD/PLAY COUNTER 7800
MEMORY WRITE LINE
PCB 15018-2
J7
P20
A29 PIN 2
P20 PIN 2
P20 PIN 1
P9 PIN 10
+12V
PCB/15015-2
HALL EFFECT INPUT
A1 74LS157
A2 74LS157
A3 QUAD 2 to 1 line MULT 74LS157
A4 74LS244
A5 74LS244
A6 74LS157
A7
A8 74LS123
74LS06
GOES LOW WHEN EITHER LAD1, TAD2, OR TAD1 IS ENABLED
SELECT 1=#
TO MEM 7800 W
DATA TRANS PULSE
+5V
.47 C4
10K R8
R13 680
C5 500
680 R11
R15 680
10K R6
R3 10K
C1 500
C2 500
C3 500 *
C6 470pF
R10 390
470 R11
R1 10K
R2 10K
Q1 2N3566
Q2 2N3566
D1 1N4446
K1
AROMAT HA1-DC12V
VCO 7800 R/P IN
PCB # 15321-3
R/P 7800
CABLE ASSY
PCB/15020-2
PCB/15015-2
J12
A5 PIN 1
A5 PIN 2
A5 PIN 3
A5 PIN 4
A5 PIN 5
A5 PIN 6
A5 PIN 7
A5 PIN 8
A5 PIN 9
A5 PIN 10
A21 A20 A19 A18 A17 A16 A15 A14 A13 A12
FROM A/D
ML MT COUNTER ADVANCE FROM A41 PIN 11 7812 TAD2
TO A30 PIN 6 7812 ML/MT
TO A12 PIN 2 7812 (DT)
FROM A12 PIN 6 7812 (DT)
FROM A12 PIN 4 7812 (DT)
TO A13 PIN 4 7812 (DT)
FROM A30 PIN 33 7812
TO A29 PIN 44 7812 TAD2
CABLE ASSY
R/P 7800
CABLE ASSY
PCB/ 15015-2
+5V
PCB # 15321-3
NC
COUNTER PCB TO 15018 P1-B16 19.2 KHz
PCB # 15531-3
* DENOTES FACTORY SELECT R15, C6

ML = MEMORY LISTEN
MT = MEMORY TALK
DT = DATA TALK

ALL RESISTORS ARE IN OHMS, 1/4W, 5% UNLESS NOTED OTHERWISE
ALL CAPACITORS ARE IN pF UNLESS NOTED OTHERWISE

BUFFER BOARD IEEE-488 INTERFACE MO #2 7812

MAT. —//— FINISH: —//— SCALE: —//—

TOLERANCES UNLESS OTHERWISE SPECIFIED:
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± 30 MIN.

CHANGE	DATE	APP.
"B" ADDED PULL RESISTORS + CAP	5/12/83	R.S.
"C" ECN 2095 RVS PR of 15321 PIN #s	6-1-83	JF
"D" ECN 2093	6-29-83	JF
"E" ECN 2105	7-20-83	JF
"F" ECN 2162	4-27-84	RM
"G" Changed C4	5-6-84	RM

KAY ELEMETRICS CORP
PINE BROOK, N. J.

DWN. BY [illegible] DATE 3-24-83
APP. BY R [illegible] DATE 3-24-83

DWG. NO. C 15531-3G

BRUNING 44-131 22990

FAIRCHILD
A Schlumberger Company

96LS488
General Purpose Interface Bus (GPIB) Circuit

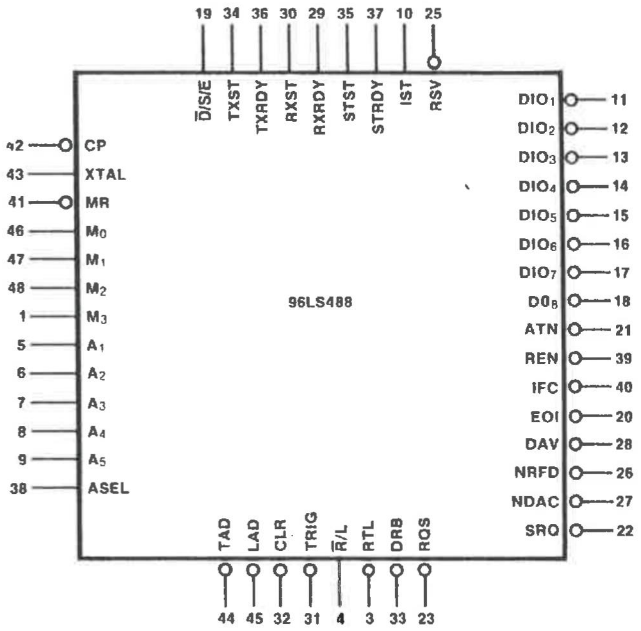
Digital Integrated Circuits

The 96LS488 is a TTL LSI circuit containing all of the logic necessary to interface Talk, Listen and Talk/Listen type instruments and system components in accordance with the IEEE-488 standard for programmable instrumentation. All outputs that drive the IEEE-488 bus are guaranteed to sink 48 mA, and all bus inputs have Schmitt triggers and bus terminating networks. All pins that interface to the instrument logic are LSTTL compatible.

The 96LS488 has programming inputs that determine whether it is to be a talker, listener or both, single or dual address, high or low speed, etc., according to the instrument and system requirements. It operates with a minimum of external support logic and readily interfaces with most microprocessors. It operates from a single 5.0 V supply and a 10 MHz single phase clock and is capable of operating the bus handshake at the full 1 MHz data rate. It offers a variety of handshaking and status connections to the instrument logic for versatility and ease of design.

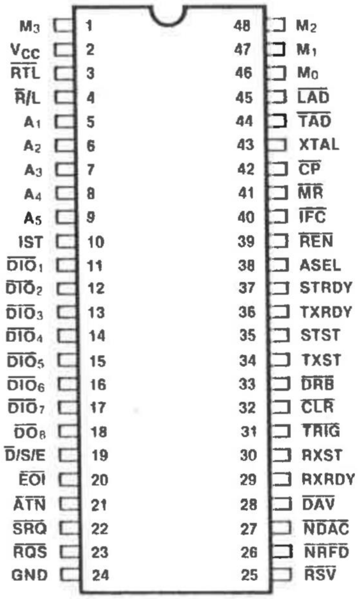
- SINGLE 5.0 V SUPPLY
- COMPLETE SOURCE AND ACCEPTOR HANDSHAKE LOGIC
- SAME OR SEPARATE TALK AND LISTEN ADDRESS
- SECONDARY ADDRESS CAPABILITY
- TALK ONLY OR LISTEN ONLY CAPABILITY
- SOURCE HANDSHAKE DELAY PROGRAMMABLE FOR LOW OR HIGH SPEED
- SERIAL POLL CAPABILITY
- PARALLEL POLL CAPABILITY
- SYNC TRIGGER AND DEVICE CLEAR OUTPUTS
- IMPLEMENTS REMOTE/LOCAL FUNCTION
- ON-CHIP CLOCK OSCILLATOR
- SERVICE REQUEST INTERRUPT FACILITY
- ALL BUS I/O SIGNALS COMPLY WITH THE IEEE-488 (1980) AND IEC-625-1 INPUT THRESHOLD, TERMINATION AND OUTPUT SPECIFICATIONS
- ALL INSTRUMENT INTERFACE SIGNALS ARE LSTTL COMPATIBLE
- GPIB PINS PRESENT NO ELECTRICAL LOAD WHEN DEVICE IS POWERED OFF

Logic Symbol


19 34 36 30 29 35 37 10 25
D/S/E
TXST
TXRDY
RXST
RXRDY
STST
STRDY
IST
RSV
42 CP
43 XTAL
41 MR
46 M0
47 M1
48 M2
1 M3
5 A1
6 A2
7 A3
8 A4
9 A5
38 ASEL
96LS488
DIO1 11
DIO2 12
DIO3 13
DIO4 14
DIO5 15
DIO6 16
DIO7 17
DO8 18
ATN 21
REN 39
IFC 40
EOI 20
DAV 28
NRFD 26
NDAC 27
SRQ 22
TAD
LAD
CLR
TRIG
R/L
RTL
DRB
ROS
44 45 32 31 4 3 33 23

V_{CC} = Pin 2
Gnd = Pin 24

Connection Diagram
48-Pin DIP


M3 1
VCC 2
RTL 3
R/L 4
A1 5
A2 6
A3 7
A4 8
A5 9
IST 10
DIO1 11
DIO2 12
DIO3 13
DIO4 14
DIO5 15
DIO6 16
DIO7 17
DO8 18
D/S/E 19
EOI 20
ATN 21
SRQ 22
ROS 23
GND 24
48 M2
47 M1
46 M0
45 LAD
44 TAD
43 XTAL
42 CP
41 MR
40 IFC
39 REN
38 ASEL
37 STRDY
36 TXRDY
35 STST
34 TXST
33 DRB
32 CLR
31 TRIG
30 RXST
29 RXRDY
28 DAV
27 NDAC
26 NRFD
25 RSV

(Top View)

Fairchild Camera and Instrument Corporation
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June, 1981 Fairchild reserves the right to make changes in the circuitry or specifications at any time without notice.

Input Loading/Fan-Out

Pin Names	Description	96LS (U.L.)** HIGH/LOW
A_1–A_5	Address Inputs	0.5/0.25
$\overline{ATN}$	Attention Input (Active LOW)	T*/1.4
$\overline{CP}$	Clock Input (Active Falling Edge)	0.5/0.25
$\overline{IFC}$	Interface Clear Input (Active LOW)	T*/1.4
IST	Instrument Status Input	0.5/0.25
$M_0 - M_3$	Mode Control Inputs	0.5/0.25
$\overline{MR}$	Master Reset Input (Active LOW)	0.5/0.25
$\overline{REN}$	Remote Enable Input (Active LOW)	T*/1.4
$\overline{RSV}$	Request Service Input (Active LOW)	0.5/0.25
$\overline{RTL}$	Return to Local Input (Active LOW)	0.5/0.25
RXRDY	Receiver Ready Input (Active HIGH)	0.5/0.25
STRDY	Status Ready Input (Active HIGH)	0.5/0.25
TXRDY	Transmitter Ready Input (Active HIGH)	0.5/0.25
$\overline{DAV}$	Data Valid Input (Active LOW)	T*/1.4
	as Output (Active LOW)	130/30
$\overline{DIO_1}$-$\overline{DIO_7}$	Data Inputs	T*/1.4
	as Outputs (Active LOW)	T*/30
$\overline{DO_8}$	Data Output (Active LOW)	T*/30
$\overline{EOI}$	End or Identify Input (Active LOW)	T*/1.4
$\overline{NDAC}$	Not Data Accepted Input (Active LOW)	T*/1.4
	as Output (Active LOW)	T*/30
$\overline{NRFD}$	Not Ready for Data Input	T*/1.4
	as Output (Active LOW)	T*/30
ASEL	Address Select Output	10/5.0 (2.5)
$\overline{CLR}$	Device Clear Output (Active LOW)	10/5.0 (2.5)
$\overline{D}$/S/E	Data/Status Output (Active LOW)	10/5.0 (2.5)
	End-of-String Output (Active HIGH)	10/5.0 (2.5)
$\overline{DRB}$	Bus Drive Enable Output (Active LOW)	10/5.0 (2.5)
$\overline{LAD}$	Listen Address Status Output (Active LOW)	10/5.0 (2.5)
$\overline{RQS}$	Requested Service Status Output (Active LOW)	130/30
RXST	Receiver Strobe Output (Active HIGH)	10/5.0 (2.5)
$\overline{R}$/L	Remote/Local Output	10/5.0 (2.5)
$\overline{SRQ}$	Service Request Output (Active LOW)	T*/30
STST	Status Strobe Output (Active HIGH	10/5.0 (2.5)
$\overline{TAD}$	Talk Address Status Output (Active LOW)	10/5.0 (2.5)
TXST	Transmitter Strobe Output (Active HIGH)	10/5.0 (2.5)
$\overline{TRIG}$	Device Trigger Output (Active LOW)	10/5.0 (2.5)
XTAL	Crystal Output	10/5.0 (2.5)

*T = Resistive Termination per IEEE-488 Standard.

**Unit Load (U.L.) definitions
LOW State: 1.6 mA = 1 U.L.
HIGH State: 40 μA = 1 U.L.

Where two sets of output LOW loading factors are shown, the one in parentheses applies over the Military V_{CC} and temperature ranges.

GPIB Protocol

A full description and specification of the GPIB system is published in the IEEE document 'IEEE Standard Interface for Programmable Instrumentation" IEEE Std 488–1978 and is used as the reference in this description.

The standard is a 16-wire interface that can transmit byte serial data at rates of up to 1 megabyte/second. Using this standard up to 15 individual devices (instruments or system components) may be interconnected in a star or linear network, with a maximum cable length of 20 m and automatically controlled or programmed. Data may be exchanged between instruments or between a controller and instruments. The use of a bus extender or a controller which can handle a number of separate instrument buses allows more than 15 instruments to be used in a system:

> Talkers—These instruments can only transmit data (when addressed), e.g., a timer or counter.
>
> Listeners—These instruments can only receive information, e.g., a programmable power supply or a printer.
>
> Talker/Listeners—These instruments can receive data or functional instructions and later transmit data, e.g., a programmable DVM or multichannel a/d converter.
>
> Controller—A device that is able to generate control instructions for instruments on the bus, e.g., a mini-computer or programmable calculator.

The 96LS488 is designed for use in any of the first three types of devices.

The 16-wire bus is organized as 3 functional groups *(Figure 1).* The 8-line Data bus, $\overline{\text{DIO}_1}$–$\overline{\text{DIO}_7}$, $\overline{\text{DO}_8}$, is used to transfer commands in bit parallel/byte serial form from Talkers to Listeners. The 3-line Data Byte Transfer Control bus, $\overline{\text{NRFD}}$, $\overline{\text{NDAC}}$ and $\overline{\text{DAV}}$, implements a data handshake which ensures that information transfer proceeds as fast as the device will allow but no faster than the slowest device currently addressed as active *(Figure 2).* The 5-line General Interface Management bus $\overline{\text{ATN}}$, $\overline{\text{REN}}$, $\overline{\text{EOI}}$, $\overline{\text{IFC}}$ and $\overline{\text{SRQ}}$ is principally used by the Controller.

In its simplest configuration the GPIB can consist of only two instruments, a Talker and a Listener; in its most complex configuration up to 961 instruments could be controlled by one or more mini-computers. A bus controller dictates the role of each device by making the $\overline{\text{ATN}}$ line LOW and sending Talk and/or Listen Addresses on the bus data lines. Those devices with matching addresses are activated accordingly. Device addresses are set by switches or PC board jumpers. In single address mode each device has a 5-bit address allowing up to 31 different addresses (one code is used as an unaddress command). In extended address mode each device has a 10-bit address, allowing up to 961 different addresses and the Controller must send two bytes in order to activate a device.

In the configuration shown in *Figure 1* a sequence to initiate a data transfer from device A to device D would proceed as follows:

> Controller sends $\overline{\text{ATN}}$ (attention) command; whenever the $\overline{\text{ATN}}$ line goes LOW, devices using the Data bus immediately stop all operations. The Controller keeps the $\overline{\text{ATN}}$ line LOW during the remainder of this sequence.
>
> Controller sends UNL (unlisten) command; this instruction disables any devices that are in Listen mode.
>
> Controller sends Talk Address command to device A; this instruction puts device A into Talk mode and disables any other devices that had been in that mode.
>
> Controller sends Listen Address command to device D, putting it in Listen mode.

When the Controller stops sending $\overline{\text{ATN}}$, the bus will be released for data transfer functions and device A will begin transmitting to device D.

The $\overline{\text{SRQ}}$ line allows any device to interrupt the Controller and request service. The Controller can identify the interrupting devices by conducting a Serial Poll. To do this it issues an Unlisten (UNL) command followed by a Serial Poll Enable (SPE) command and then the Talk Address of each device in turn. The interrupting device will optionally drive $\overline{\text{DIO}_7}$ LOW. Alternatively the Controller can conduct a Parallel Poll by making both $\overline{\text{EOI}}$ and $\overline{\text{ATN}}$ LOW. Devices will then return one bit of status on a $\overline{\text{DIO}}$ line previously assigned via a Parallel Poll Enable (PPE) command.

The $\overline{\text{REN}}$ line allows the Controller to put all Listen addressed instruments into remote control mode, while the $\overline{\text{IFC}}$ line allows the Controller to initialize the system.

Fig. 1 Interface Capabilities and Bus Structure

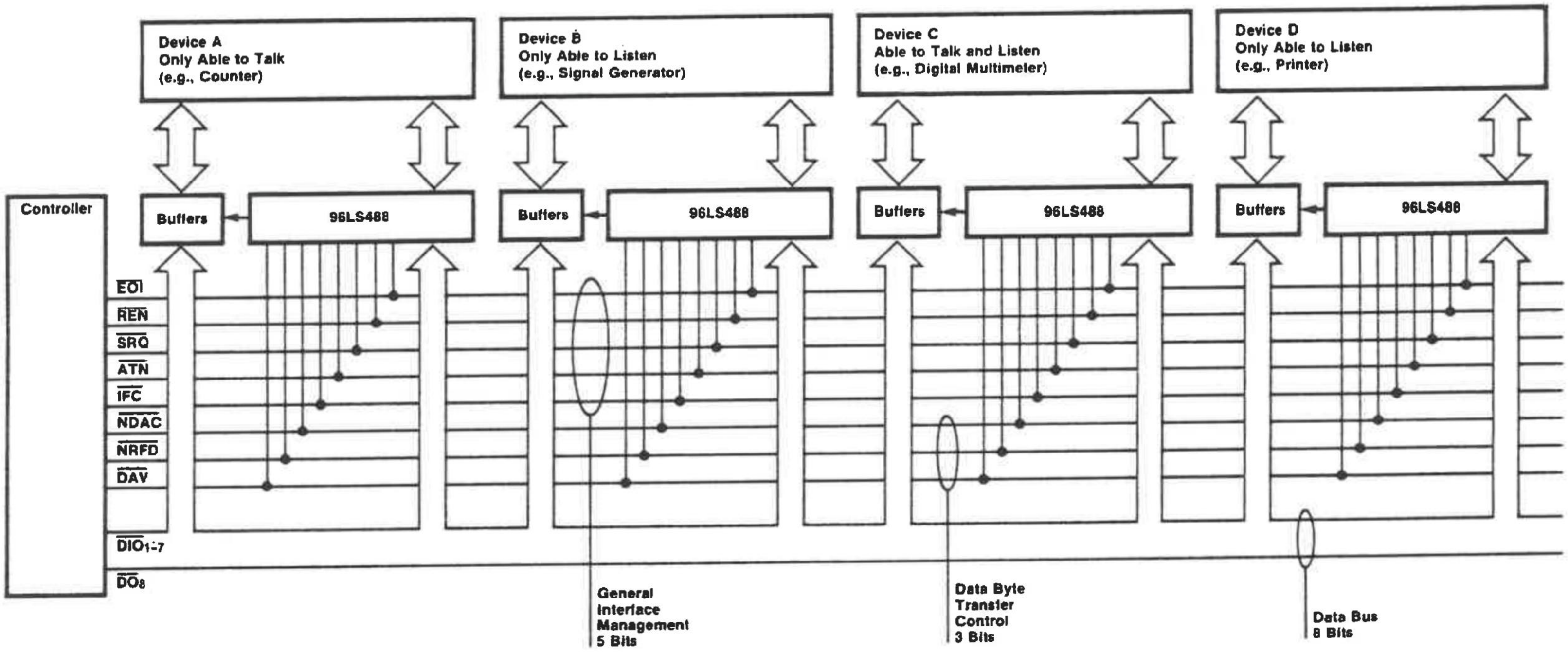
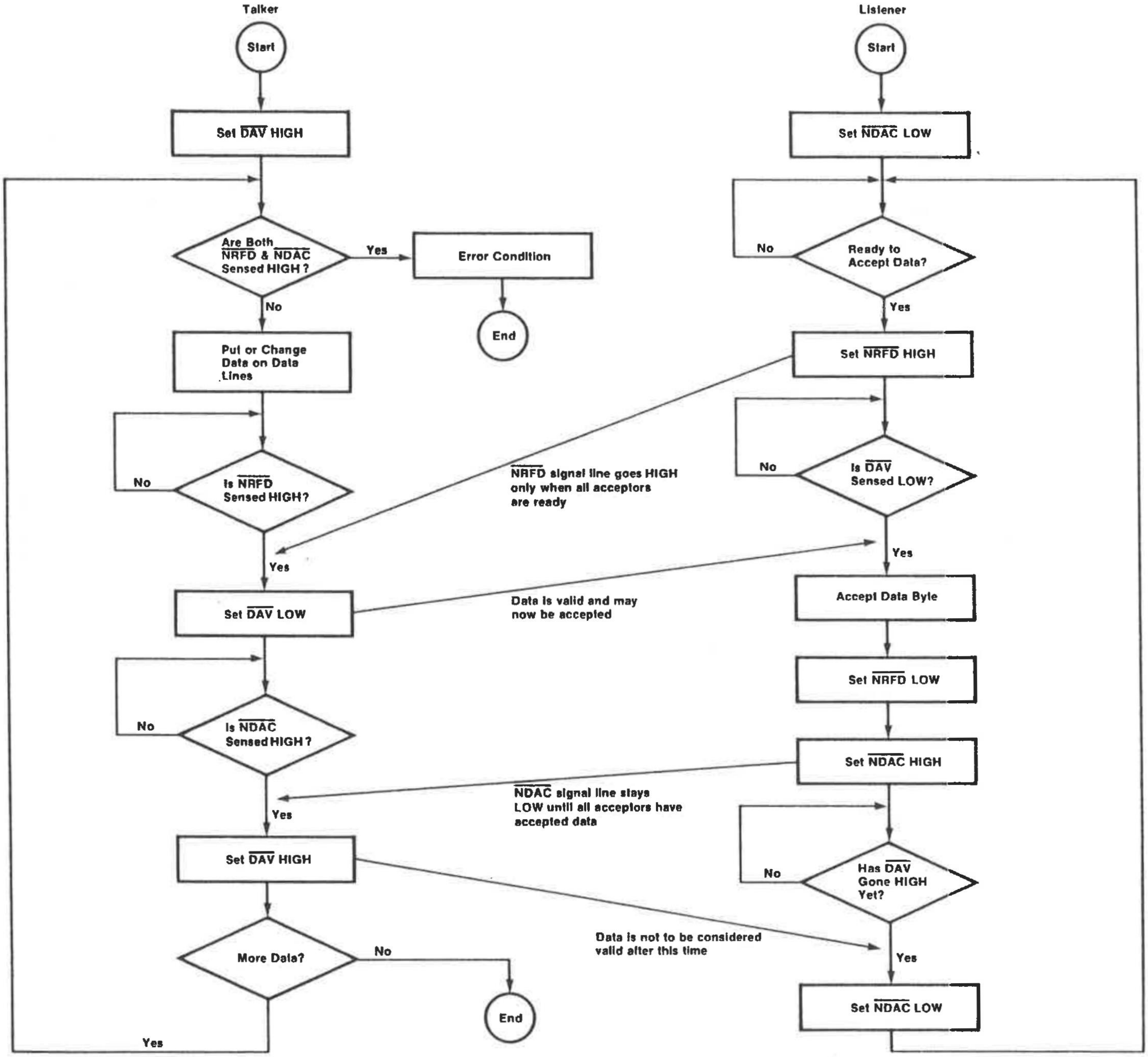
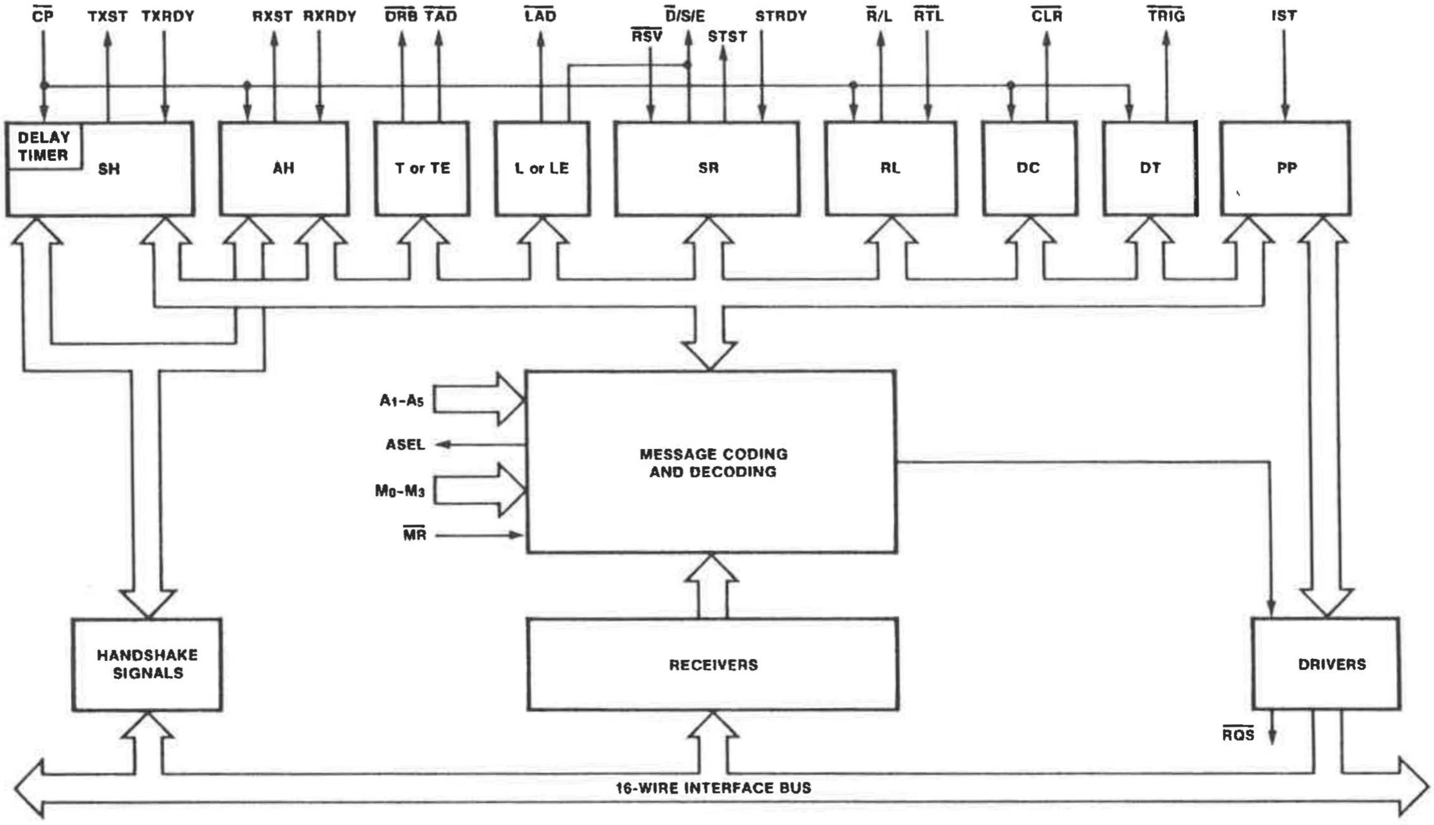

Device A
Only Able to Talk
(e.g., Counter)
Device B
Only Able to Listen
(e.g., Signal Generator)
Device C
Able to Talk and Listen
(e.g., Digital Multimeter)
Device D
Only Able to Listen
(e.g., Printer)
Controller
Buffers
96LS488
$\overline{EOI}$
$\overline{REN}$
$\overline{SRQ}$
$\overline{ATN}$
$\overline{IFC}$
$\overline{NDAC}$
$\overline{NRFD}$
$\overline{DAV}$
$\overline{DIO}_{1-7}$
$\overline{DO}_8$
General Interface Management 5 Bits
Data Byte Transfer Control 3 Bits
Data Bus 8 Bits

Fig. 2 Source and Acceptor Handshake Logic


Talker
Start
Set $\overline{DAV}$ HIGH
Are Both $\overline{NRFD}$ & $\overline{NDAC}$ Sensed HIGH ?
Yes
Error Condition
End
No
Put or Change Data on Data Lines
No
Is $\overline{NRFD}$ Sensed HIGH?
Yes
Set $\overline{DAV}$ LOW
No
Is $\overline{NDAC}$ Sensed HIGH ?
Yes
Set $\overline{DAV}$ HIGH
More Data?
No
End
Yes
Listener
Start
Set $\overline{NDAC}$ LOW
No
Ready to Accept Data?
Yes
Set $\overline{NRFD}$ HIGH
No
Is $\overline{DAV}$ Sensed LOW?
Yes
Accept Data Byte
Set $\overline{NRFD}$ LOW
Set $\overline{NDAC}$ HIGH
No
Has $\overline{DAV}$ Gone HIGH Yet?
Yes
Set $\overline{NDAC}$ LOW
$\overline{NRFD}$ signal line goes HIGH only when all acceptors are ready
Data is valid and may now be accepted
$\overline{NDAC}$ signal line stays LOW until all acceptors have accepted data
Data is not to be considered valid after this time

96LS488 Functional Block Diagram


$\overline{\text{CP}}$
TXST
TXRDY
RXST
RXRDY
$\overline{\text{DRB}}$
$\overline{\text{TAD}}$
$\overline{\text{LAD}}$
$\overline{\text{D}}$/S/E
$\overline{\text{RSV}}$
STST
STRDY
$\overline{\text{R}}$/L
$\overline{\text{RTL}}$
$\overline{\text{CLR}}$
$\overline{\text{TRIG}}$
IST
DELAY TIMER
SH
AH
T or TE
L or LE
SR
RL
DC
DT
PP
A_1-A_5
ASEL
M_0-M_3
$\overline{\text{MR}}$
MESSAGE CODING AND DECODING
HANDSHAKE SIGNALS
RECEIVERS
DRIVERS
$\overline{\text{RQS}}$
16-WIRE INTERFACE BUS

Functions Implemented by the 96LS488

Acceptor Handshake (AH)
Controls the acquisition of addresses, interface commands and data bytes from the bus. The AH passes data bytes to the instrument logic via a 2-wire handshake (RXST, RXRDY) and a status output ($\overline{\text{LAD}}$).

Source Handshake (SH)
Controls the passing of data bytes and status information from the instrument to the bus. The SH communicates with the instrument via a 2-wire handshake (TXST, TXRDY) and a status output ($\overline{\text{TAD}}$). It has two operating speeds, selectable via the M_0-M_3 inputs. Low speed is used with open collector data drivers and gives a settling delay of 2.0 μs. High speed is used with 3-state bus drivers and gives a settling delay of 1.1 μs for the first byte sent and 0.5 μs for the subsequent bytes (clock frequency 10 MHz).

Listener, Extended Listener (L or LE)
Either the single or extended address L function can be selected by the M_0-M_3 inputs. The 96LS488 flags the listener addressed status via the $\overline{\text{LAD}}$ output. The listen address is defined by the A_1-A_5 inputs and, where the extended address feature is used, the ASEL output controls an external multiplexer to select the primary or secondary address as required.

Talker, Extended Talker (T OR TE)
Either the single or extended address T function can be selected. The T function employes the M_0-M_3 and A_1-A_5 inputs in the same manner as the L function. The 96LS488 flags the talker addressed status via the $\overline{\text{TAD}}$ output. The T function also incorporates the Serial Poll Function.

Talker/Listener, Extended Talker/Listener
For instruments with both talk and listen capabilities, the 96LS488 implements both the T and L functions. In this mode, the "Untalk if My Listen Address" and "Unlisten if My Talk Address" feature is standard. Where the single address mode is selected, different Talk and Listen addresses can be used. In the extended address mode, the Talk and Listen addresses must be identical.

Device Trigger, Device Clear (DT, DC)
These functions generate a pulse on the Trigger or Clear output upon receipt of the relevant bus command.

Remote Local (RL)
The complete RL function is implemented, including the Local Lock-Out feature.

Talk Only, Listen Only
The 96LS488 can operate in either of these two modes via the M_0-M_3 input code selection.

Service Request (SR)
The 96LS488 initiates an SR on receipt of the $\overline{\text{RSV}}$ input and returns its status on the $\overline{\text{RQS}}$ line when serial polled. The $\overline{\text{RQS}}$ output can be used to drive the $\overline{\text{DIO}}_7$ bus line directly.

Parallel Poll (PP)
The Controller assigns, via the PPE command, one of the eight data lines for use as the Parallel Poll Response output. When the Controller issues the IDY command, the 96LS488 compares the state of the IST input with the state defined by the last PPE command. If the comparison is True, the previously assigned $\overline{\text{DIO}}$ line is driven LOW by the 96LS488.

Pin Functions

488 Bus Signals
All bus inputs have Schmitt trigger buffers, and all bus outputs can sink 48 mA. Each bus signal is terminated with a resistive load and meets the dc load characteristics specified in section 3.5.3 of the IEEE Std 488 – 1978 specification.

$\overline{\text{DIO}}_1$-$\overline{\text{DIO}}_7$ (Data Input/Output)—These are used as inputs to receive addresses and interface commands. They are used as outputs, along with $\overline{\text{DO}}_8$ to provide Parallel Poll response.

$\overline{\text{ATN}}$ (Attention)—This is an input from the GPIB Controller. When $\overline{\text{ATN}}$ is LOW the 96LS488 interprets the data on $\overline{\text{DIO}}_1$-$\overline{\text{DIO}}_7$ lines as commands or addresses. If the 96LS488 is interrupted by $\overline{\text{ATN}}$ while sending data, it will relinquish control of the Data and Management lines within 200 ns.

$\overline{\text{DAV}}$ (Data Valid)—A bidirectional signal with a 3-state output driver, $\overline{\text{DAV}}$ is part of the handshake system and is driven LOW by current talker when a valid data byte, command or address is on the GPIB. $\overline{\text{DAV}}$ is treated as an input when the 96LS488 is addressed to Listen, or is receiving $\overline{\text{ATN}}$. It is an output when the 96LS488 is addressed to Talk and $\overline{\text{ATN}}$ is HIGH.

$\overline{\text{NRFD}}$ (Not Ready for Data)—A bidirectional signal with an open-collector output driver, $\overline{\text{NRFD}}$ is part of the handshake system and is driven LOW to indicate that an instrument is not ready to receive data. The 96LS488 drives $\overline{\text{NRFD}}$ HIGH when addressed as a Listener and the instrument is ready to accept a data byte or when $\overline{\text{ATN}}$ is LOW and the 96LS488 is ready to accept an address or interface command. $\overline{\text{NRFD}}$ is treated as an input when the 96LS488 is addressed to Talk.

$\overline{\text{NDAC}}$ (Not Data Accepted)—A bidirectional signal with an open-collector output driver, $\overline{\text{NDAC}}$ is part of the handshake system and is pulled LOW to indicate that a device has not yet accepted a data byte. $\overline{\text{NDAC}}$ is treated as an input when the 96LS488 is addressed to Talk. It is an output and is driven LOW when the 96LS488 is addressed to Listen and the instrument has not accepted a data byte or when receiving $\overline{\text{ATN}}$ and the 96LS488 has not accepted an address or interface command.

$\overline{\text{SRQ}}$ (Service Request)—This is an open-collector output driven LOW when the instrument requests service (via $\overline{\text{RSV}}$) from the Controller.

$\overline{\text{RQS}}$ (Requested Service)—A 48 mA 3-state output, enabled during a Serial Poll response and driven LOW if the 96LS488 initiated an $\overline{\text{SRQ}}$, $\overline{\text{RQS}}$ can be directly connected to $\overline{\text{DIO}}_7$ in applications where it is the only status information to be sent.

$\overline{\text{EOI}}$ (End or Identify)—This is an input from the GPIB Controller used to elicit a Parallel Poll response, or from the current active talker to indicate the End-of-string (END) message.

$\overline{\text{REN}}$ (Remote Enable)—This is an input driven by the Controller. The Controller drives it LOW when it needs to remotely program an instrument.

$\overline{\text{IFC}}$ (Interface Clear)—This is an input from the Controller, driven LOW to clear the interface logic. (See *Figure 18.*)

Instrument Interface and Auxiliary Pins
Instrument Logic Signals—All instrument logic signals are standard low-power Schottky compatible.

$\overline{\text{CP}}$ (10 MHz Clock)—Used to clock internal-state flip-flops and is divided down internally to generate the SH data settling delay. All output changes are synchronous with the negative clock edge. The $\overline{\text{CP}}$ input can be driven by an external oscillator or used in conjunction with XTAL output, as an RC or a crystal oscillator. (See *Figure 6.*)

XTAL (Crystal)—Used to connect a crystal or external RC timing components for the on-chip oscillator. (See *Figure 6.*)

$\overline{\text{MR}}$ (Active-LOW Master Reset)—Initializes all internal latches and is completely asynchronous. After a reset, all outputs to the GPIB are passive HIGH and $\overline{\text{RQS}}$ is in the high-Z state; $\overline{\text{R}}$/L, $\overline{\text{TRIG}}$, $\overline{\text{CLR}}$, $\overline{\text{DRB}}$, ASEL, $\overline{\text{TAD}}$ and $\overline{\text{LAD}}$ are HIGH; $\overline{\text{D}}$/S/E, RXST, STST and TXST are LOW.

M_0–M_3 (Mode Control Inputs)—Define 1 of 14 possible operating modes for the 96LS488. M_0–M_3 are HIGH-true inputs.

A_1–A_5 (Device Address Inputs)—Define the instrument address and originate from switches, PC jumpers or software-loaded register. Where different Talk and Listen addresses are required or when the secondary address feature is used, these inputs must be externally multiplexed, using the ASEL output to control the multiplexer. A_1–A_5 are HIGH-true inputs (H = 1, L = 0) and thus have the opposite polarity of the $\overline{\text{DIO}}_1$–$\overline{\text{DIO}}_5$ addresses.

ASEL (Address Select Output)—Selects, via an external multiplexer, the Talk/Listen or primary/secondary address input, depending on the operating mode selected; LOW for Talk or primary address; HIGH for Listen or secondary address. (See *Figure 11.*)

$\overline{\text{LAD}}$, $\overline{\text{TAD}}$ (Address Status Outputs)—Indicate the Listen-Address or Talk-Address status respectively. They are also activated in the Talk-Only and Listen-Only modes. The outputs are active-LOW to facilitate driving LED indicator lamps. (See *Figures 7, 10.*)

RXST (Receiver Strobe Output)—Forms part of the handshake logic to pass data bytes to the instrument. When addressed to Listen, the 96LS488 takes RXST HIGH when a valid data byte is on the bus and holds it HIGH until the instrument signals (via the RXRDY input) that it has processed the byte. RXST may be inverted and connected to RXRDY, in which case the 96LS488 will receive data bytes from the bus at a data rate determined solely by the bus handshake. (See *Figure 8.*)

TXST (Transmit Strobe Output)—Forms part of the handshake logic to pass data bytes from the instrument to the bus. When addressed to Talk, the 96LS488 takes TXST HIGH to signal the instrument that the bus has accepted the data. TXST does not go LOW again until the instrument has acknowledged that the byte has been accepted (via the TXRDY INPUT). TXST may be inverted and connected to TXRDY, in which case the 96LS488 will transmit data bytes to the bus at a data rate determined solely by the bus handshake. (See *Figure 9.*)

STST (Status Strobe Output)—Forms part of the handshake logic to pass a status byte from the instrument to the bus during a Serial Poll sequence. It operates in conjunction with the STRDY input in the same way as the TXST and TXRDY signals. STST may be inverted and connected to STRDY, in which case the status byte will be repeated as long as the 96LS488 is addressed to Talk. (See *Figure 16.*)

RXRDY (Receiver Ready Input)—Forms part of the handshake logic controlling the passing of data from the bus to the instrument. RXRDY is driven HIGH when the instrument is ready to receive a data byte and LOW to acknowledge receipt of a data byte. (See *Figure 8.*)

TXRDY (Transmitter Ready Input)—Forms part of the handshake logic controlling the passing of data from the instrument to the bus. When the 96LS488 is addressed to Talk, TXRDY is driven HIGH when the instrument has a data byte to send and LOW to acknowledge that the byte has been accepted by the bus. (See *Figure 9.*)

STRDY (Status Ready Input)—Forms part of the handshake logic controlling the passing of a status byte to the bus during a Serial Poll sequence. It operates in a similar fashion to TXRDY. (See *Figure 16.*)

$\overline{\text{RSV}}$ (Request Service Input)—Is pulled LOW by the instrument to request service and initiate an $\overline{\text{SRQ}}$ interrupt to the controller. This interrupt will be cleared if $\overline{\text{RSV}}$ goes HIGH before it is serviced, but once the $\overline{\text{SRQ}}$ is serviced, $\overline{\text{RSV}}$ must, after exiting SPAS, go HIGH then LOW to initiate another service request. (See *Figure 16.*)

$\overline{\text{CLR}}$ (Clear Output)—Issues a negative pulse when the 96LS488 receives a Device Clear (DC) command, or when it is addressed to Listen and receives a Selected Device Clear. The $\overline{\text{CLR}}$ Output will stay LOW during Accept Data State (ACDS) or until $\overline{\text{ATN}}$ goes HIGH. (See *Figure 13.*)

$\overline{\text{TRIG}}$ (Trigger Output)—Issues a negative pulse when the 96LS488 is addressed to Listen and receives a DT command. The $\overline{\text{TRIG}}$ output will stay LOW during ACDS or until $\overline{\text{ATN}}$ goes HIGH. (See *Figure 13.*)

$\overline{\text{DRB}}$ (Drive Bus Output)—Taken LOW to enable an external data bus driver when the 96LS488 is addressed to Talk and is in the Talker Active State. $\overline{\text{DRB}}$ will go LOW one clock period after $\overline{\text{ATN}}$ goes HIGH, and will go HIGH asynchronously within 200 ns (typically 70 ns) after $\overline{\text{ATN}}$ goes LOW. (See *Figures 9, 10, 11.*) $\overline{\text{DRB}}$ can also be used to tell the instrument logic to fetch the first byte.

$\overline{\text{RQS}}$ (Requested Service Output)—A 48 mA 3-state output, enabled during a Serial Poll response and driven LOW if the 96LS488 initiated an $\overline{\text{SRQ}}$. $\overline{\text{RQS}}$ can be directly connected to $\overline{\text{DIO}}_7$ in applications where it is the only status information to be sent. (See *Figures 4, 5, 16.*)

$\overline{\text{D}}$/S/E (Data/Status or END Output)—Valid during the Talk Addressed state and indicates to the instrument logic whether the information to be sent via the bus is to be data or status (LOW for data, HIGH for status). A status byte is sent only in response to a Serial Poll, and, in this case, $\overline{\text{D}}$/S/E may be used to control a multiplexer to select data or status as the source to the bus data drivers. (See *Figures 4, 5, 16.*) Valid during the Listener Active State (LACS) to indicate that the current talker is sending the END message; a HIGH output indicates that the END message is true.

$\overline{\text{R}}$/L (Remote/Local Output)—Goes LOW when the Controller puts the instrument into Remote mode via the $\overline{\text{REN}}$ command. (See *Figures 14, 15.*)

$\overline{\text{RTL}}$ (Return to Local Input)—Taken LOW to request return of the instrument to local control. $\overline{\text{RTL}}$ will set $\overline{\text{R}}$/L HIGH unless the Controller has put the 96LS488 into Local Lock-out state. (See *Figure 14.*)

IST (Instrument Status Input)—Used by the Parallel Poll logic, IST is compared with the logic state defined by $\overline{\text{DIO}}_4$ during the last PPE command. If IST is in the defined state, the 96LS488 will make an affirmative response to the next IDY message by making the assigned $\overline{\text{DIO}}$ line LOW. Note that IST is a HIGH-true input while $\overline{\text{DIO}}_4$ is LOW-true. (See *Figure 17.*)

Operating Modes

The 96LS488 has 14 operating modes, defined by a 4-bit input code M_0–M_3 which would normally be selected by switches or PC board jumpers.

Table 1 defines the input codes and operating modes.

Table 1

Mode Inputs				Operating Mode	Function
M_0	M_1	M_2	M_3		
L	L	L	L	Off Line	The device cannot take part in any GPIB operations
L	L	L	H	TON (LOW Speed)[1]	The device goes directly to the talk addressed state and can source data to the bus
L	L	H	L	LON	The device goes directly to the listen addressed state and can receive data from the bus
L	L	H	H	TON (HIGH Speed)[1]	As for TON (LOW Speed)
L	H	L	L	T (LOW Speed)[1]	Talker Only, single address mode
L	H	L	H	TE (LOW Speed)[1]	Talker Only, extended address mode
L	H	H	L	T (HIGH Speed)[1]	Talker Only, single address mode
L	H	H	H	TE (HIGH Speed)[1]	Talker Only, extended address mode
H	L	L	L	L	Listener Only, single address mode
H	L	L	H	LE	Listener Only, extended address mode
H	H	L	L	T/L (LOW Speed)[1, 2]	Talker/Listener, dual address mode
H	H	L	H	TE/LE (LOW Speed)[1]	Talker/Listener, extended address mode
H	H	H	L	T/L (HIGH Speed)[1, 2]	Talker/Listener, dual address mode
H	H	H	H	TE/LE (HIGH Speed)[1]	Talker/Listener, extended address mode

Notes

1. The LOW speed talker option is selected where open-collector data drivers are used. The delay from putting valid data on the GPIB to $\overline{\text{DAV}}$ going true is 2.0 μs. The HIGH speed option is selected where 3-state drivers are used. The settling delay (data to $\overline{\text{DAV}}$) is 1.1 μs for the first byte sent after a LOW to HIGH transition of $\overline{\text{ATN}}$ and 500 ns for subsequent bytes.
2. For dual address Talker/Listener modes the Talk and Listen addresses can be different.

Table 2

$\overline{DO_8}$	$\overline{DIO_7}$	$\overline{DIO_6}$	$\overline{DIO_5}$	$\overline{DIO_4}$	$\overline{DIO_3}$	$\overline{DIO_2}$	$\overline{DIO_1}$	
X	H	L	$\overline{A}_5$	$\overline{A}_4$	$\overline{A}_3$	$\overline{A}_2$	$\overline{A}_1$	Primary Listen Address
X	H	L	L	L	L	L	L	Unlisten
X	L	H	$\overline{A}_5$	$\overline{A}_4$	$\overline{A}_3$	$\overline{A}_2$	$\overline{A}_1$	Primary Talk Address
X	L	H	L	L	L	L	L	Untalk
X	L	L	$\overline{S}_5$	$\overline{S}_4$	$\overline{S}_3$	$\overline{S}_2$	$\overline{S}_1$	Secondary Address

Addresssing Modes

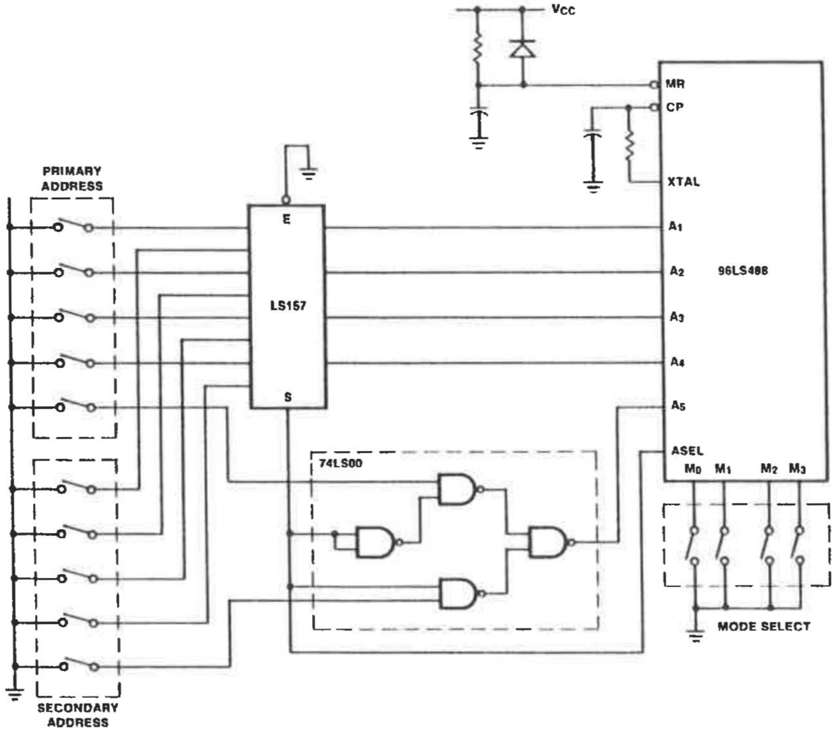
Where extended addressing or different Talk and Listen addresses are required, the address codes must be externally multiplexed, using ASEL. (See *Figure 3.*) In the extended address modes, ASEL is LOW for the primary address and HIGH for the secondary address. (See *Figure 11.*) In the dual address modes, ASEL is HIGH for the Listen address and LOW for the Talk address.

In single address mode the 96LS488 will go into the addressed state on receipt of the primary address. In extended address mode it will go to the addressed state on receipt of its secondary address if, and only if, it has received its primary address. If a device is addressed to Talk and receives its Listen address it will un-address as a Talker and go to Listener addressed state, and vice versa. A Talker Addressed device will un-address if it receives a non-matching talk address. The 96LS488 indicates its address status on the $\overline{TAD}$, $\overline{LAD}$ and $\overline{D}$/S/E outputs. (See *Table 3.*)

Table 3
Status Codes

$\overline{TAD}$	$\overline{LAD}$	$\overline{D}$/S/E	State
H	H	L	Off Line
H	L	L	Addressed to Listen (LADS)
L	H	L	Addressed to Talk (TADS)
L	H	H	Serial Poll Mode (SPM)
H	L	H	Receiving END Message (LACS)

Fig. 3 Address Multiplexer



Status Response

In Serial Poll Active State (SPAS) the instrument is requested to return a status byte, via the usual handshake, to the Controller. Seven bits are defined by the instrument. Bit 7 denotes the Request Service Status ($\overline{\text{RQS}}$) and is provided by the 96LS488 on the $\overline{\text{RQS}}$ output. If the instrument provides no status, other than $\overline{\text{RQS}}$, then the $\overline{\text{RQS}}$ output can drive the bus directly *(Figure 4)*. If the instrument provides status information this can be multiplexed to the bus using $\overline{\text{D}}$/S/E *(Figure 5)*. After the bus handshake, the instrument can send a second status byte by making STRDY LOW then HIGH again, which starts the handshake. This sequence can be repeated to send additional bytes, as long as $\overline{\text{ATN}}$ remains HIGH. *(Figure 16.)*

Fig. 4 Status Bit Driven Direct by RQS

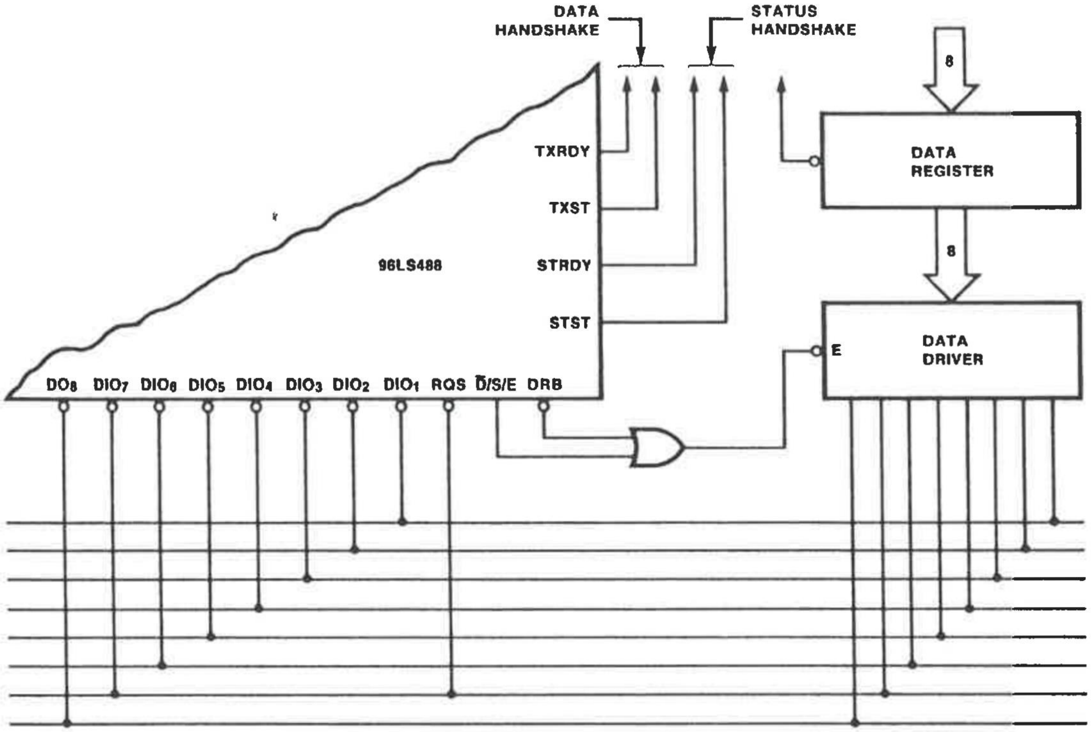
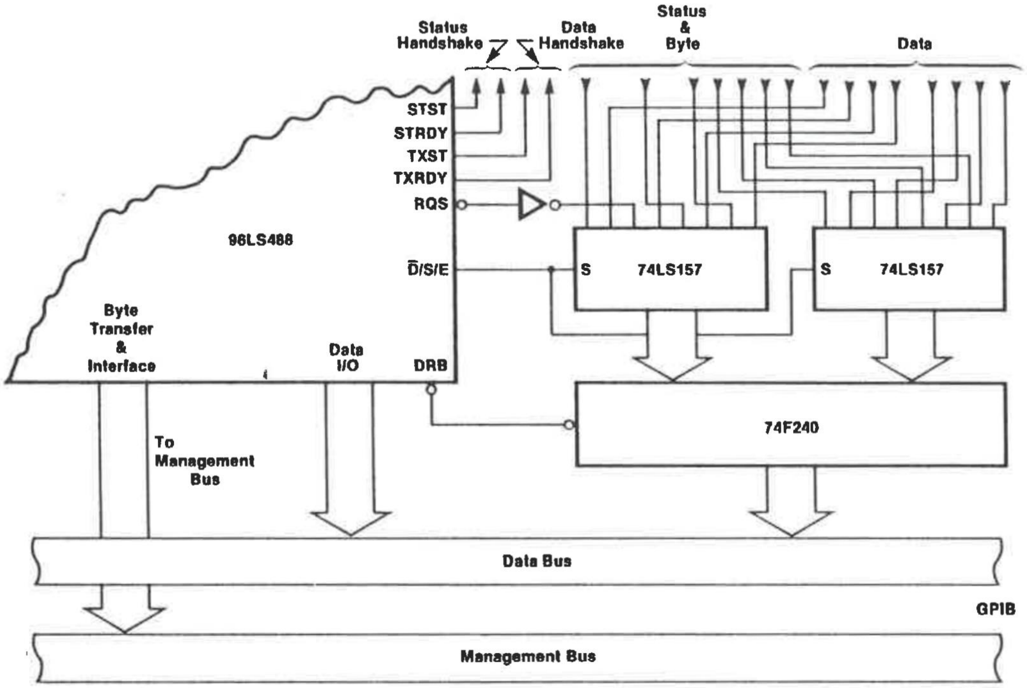

DATA HANDSHAKE
STATUS HANDSHAKE
8
DATA REGISTER
8
DATA DRIVER
E
TXRDY
TXST
96LS488
STRDY
STST
DO8
DIO7
DIO6
DIO5
DIO4
DIO3
DIO2
DIO1
RQS
D/S/E
DRB

Fig. 5 Status Byte Multiplexing


Status Handshake
Data Handshake
Status & Byte
Data
STST
STRDY
TXST
TXRDY
RQS
96LS488
D/S/E
S
74LS157
S
74LS157
Byte Transfer & Interface
Data I/O
DRB
74F240
To Management Bus
Data Bus
GPIB
Management Bus

Clock Input

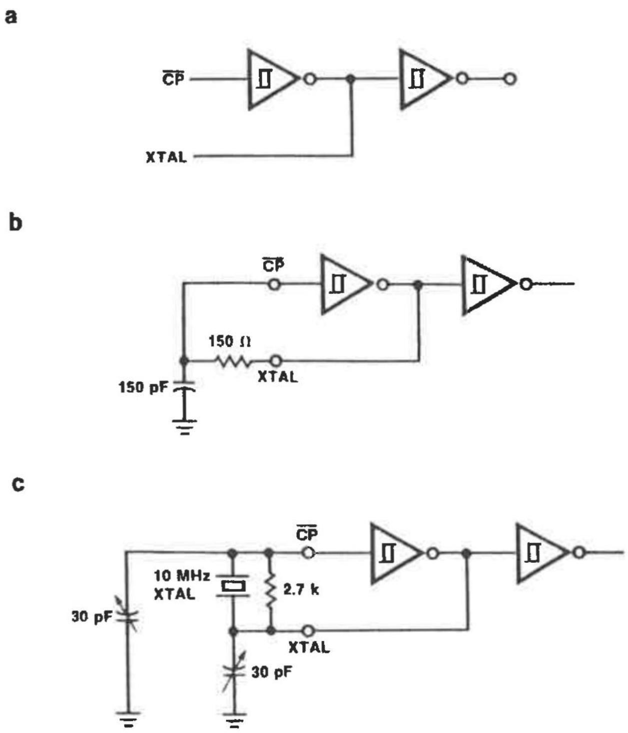
The $\overline{CP}$ and XTAL inputs allow the 96LS488 either to accept external clock pulses or to generate its own clock. (See *Figure 6*.)

(a) An external clock can drive $\overline{CP}$. The XTAL pin may be used as an inverted buffered version of the external clock.

(b) The Schmitt-trigger buffer-inverter between the $\overline{CP}$ and XTAL pins can be used as a relaxation oscillator by connecting an RC network to provide feedback. The frequency of oscillation is variable up to 10 MHz. XTAL may be used to clock external circuits provided it is buffered.

(c) The $\overline{CP}$ and XTAL pins will form a stable crystal oscillator by connecting a 10 MHz crystal and an RC network to provide positive feedback. XTAL may be used to clock external circuits provided it is buffered.

Fig. 6 Clock Timing Component Connections


a
CP
XTAL
b
CP
150 Ω
XTAL
150 pF
c
CP
10 MHz XTAL
2.7 k
30 pF
XTAL
30 pF

Timing Sequences

A 10 MHz clock frequency is recommended to give the correct Source Handshake delays. The 96LS488 can be clocked at a slower rate if the GPIB is not running at its maximum data rate of 1M byte. The lowest clock frequency allowable is dependent on the GPIB speed.

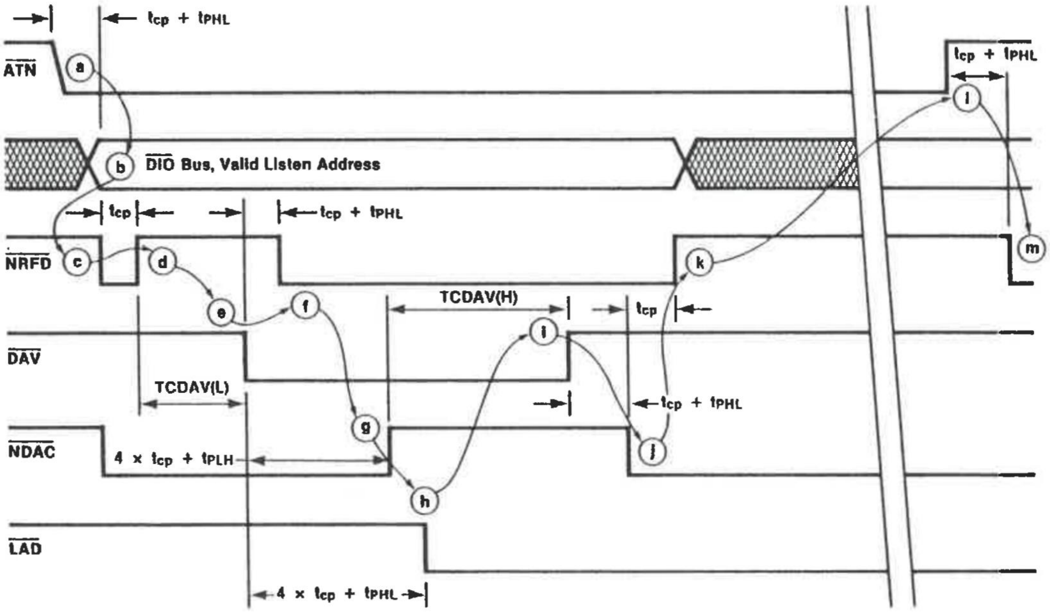
Regardless of clock frequency, the 96LS488 will respond to $\overline{\text{ATN}}$ within 200 ns by disabling $\overline{\text{NRFD}}$, $\overline{\text{NDAC}}$ and $\overline{\text{DAV}}$ while forcing $\overline{\text{DRB}}$ HIGH to disable the data drivers. In Parallel Poll sequences the relevant $\overline{\text{DIO}}$ line will be enabled or disabled within 200 ns of an IDY transition.

Since the internal logic of the 96LS488 is synchronous with the $\overline{\text{CP}}$ input, while in general all inputs are asynchronous, the precise timing of all responses to external signals is subject to a maximum uncertainty equal to one clock period. This is illustrated in the following timing diagrams, where some delays are defined as $t_{cp} + t_x$ (i.e., clock period + propagation delay).

Listen Address Sequence (See *Figure 7*)

a. Controller takes $\overline{\text{ATN}}$ line LOW followed by
b. putting the Listen address on the GPIB
c. Within ($t_{cp} + t_{PHL}$) the 96LS488 takes $\overline{\text{NRFD}}$ and $\overline{\text{NDAC}}$ LOW
d. and a t_{cp} later takes $\overline{\text{NRFD}}$ HIGH, indicating that the 96LS488 is ready for data
e. After a delay TCDAV(L) (determined by the Controller logic) the Controller takes $\overline{\text{DAV}}$ LOW
f. Within ($t_{cp} + t_{PHL}$) the 96LS488 takes $\overline{\text{NRFD}}$ LOW and
g. 3 clock periods later $\overline{\text{NDAC}}$ goes HIGH, indicating that the 96LS488 has accepted the data
h. followed by $\overline{\text{LAD}}$ indicating listen addressed status
i. After a Controller dependent delay, TCDAV(H), the $\overline{\text{DAV}}$ line goes HIGH and
j. within ($t_{cp} + t_{PHL}$) the 96LS488 takes $\overline{\text{NDAC}}$ LOW
k. A t_{cp} later the 96LS488 allows $\overline{\text{NRFD}}$ to go HIGH. $\overline{\text{NRFD}}$ stays HIGH until the Controller takes $\overline{\text{ATN}}$ HIGH, unless a further command is sent over the GPIB when a similar handshake sequence takes place
l. $\overline{\text{ATN}}$ goes HIGH followed by
m. $\overline{\text{NRFD}}$ going LOW within ($t_{cp} + t_{PHL}$). This occurs if the instrument is not ready to receive data (RXRDY LOW). If RXRDY is HIGH, $\overline{\text{NRFD}}$ will stay HIGH allowing a data transfer to take place

Fig. 7 Timing Diagram for Listen Address Sequence



Note: $\overline{\text{ATN}}$, $\overline{\text{DIO}}$ Bus & $\overline{\text{DAV}}$ driven by controller
$\overline{\text{NRFD}}$, $\overline{\text{NDAC}}$ Driven by 96LS488

Data Transfer from Bus to Listener (See *Figure 8*)
Assuming the instrument logic responds to RXST within one clock period. (See *Figure 8a.*)

a. The instrument signals it is ready to receive a byte by taking RXRDY HIGH (keeping RXRDY LOW constitutes an "$\overline{\text{NRFD}}$ hold").
b. Provided the 96LS488 is in the Listen Addressed State (LADS), $\overline{\text{NRFD}}$ is taken HIGH within $(t_{cp} + t_{PHL})$
c. When the current Talker sees the $\overline{\text{NRFD}}$ line HIGH it takes $\overline{\text{DAV}}$ LOW after a settling delay TTDAV(L).
d. The 96LS488 takes RXST HIGH within $(t_{cp} + t_{PLH})$ to inform the instrument that the GPIB data is valid and takes $\overline{\text{NRFD}}$ LOW
e. Assuming the instrument responds by pulsing RXRDY LOW within one clock period $(t_{PRX} < t_{cp})$ then RXST will remain HIGH only for one clock
f. At the same time as RXST returns LOW, $\overline{\text{NDAC}}$ is taken HIGH to inform the Talker that data has been accepted
g. After a delay TTDAV(H) determined by the Talker the $\overline{\text{DAV}}$ line goes HIGH
h. Within $(t_{cp} + t_{PHL})$ $\overline{\text{NDAC}}$ goes LOW
i. Followed by $\overline{\text{NRFD}}$ going HIGH one clock later

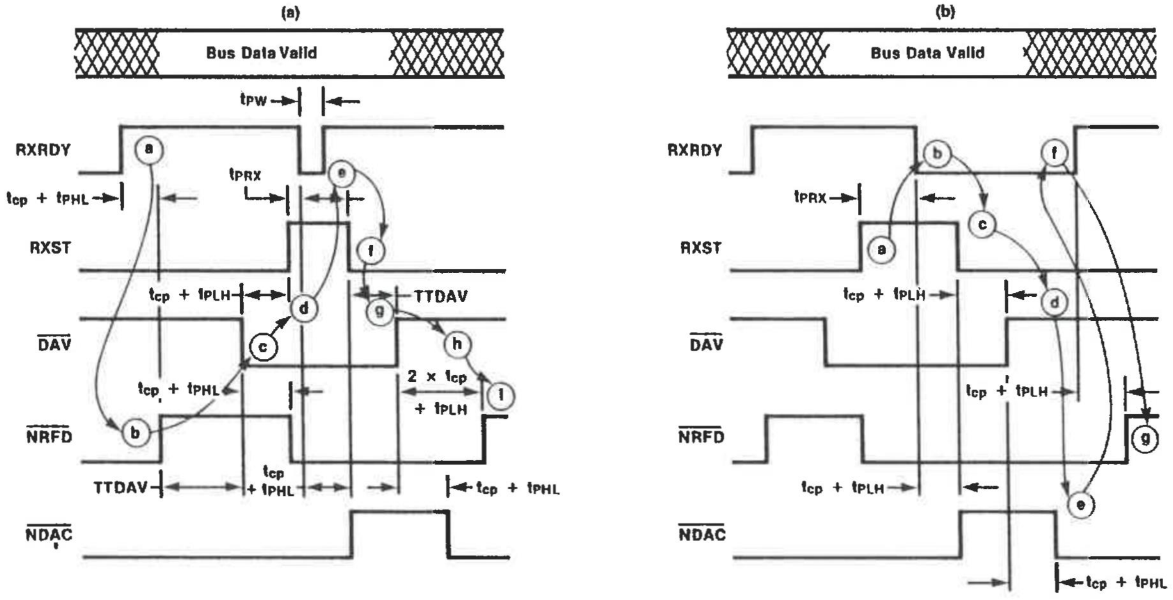
Note
In applications where the bus data can be latched by the RXST rising edge and handshaking is not necessary, RXRDY can be driven by RXST via an inverter.

Assuming the instrument logic is slow and requires more than one clock period to process a data byte. (See *Figure 8b.*)

The timing sequence is identical to *Figure 8a* until RXST goes HIGH

a. After RXST goes HIGH the instrument delays t_{PRX} (>1 clock cycle) before taking RXRDY LOW
b. RXST will remain HIGH and $\overline{\text{NDAC}}$ will remain LOW during this period, causing the bus data to be maintained valid
c. RXST goes LOW, and $\overline{\text{NDAC}}$ goes HIGH within $(t_{cp} + t_{PHL})$ of RXRDY
d. After a delay TTDAV(H) the Talker takes $\overline{\text{DAV}}$ HIGH
e. Within $(t_{cp} + t_{PHL})$ $\overline{\text{NDAC}}$ goes LOW
f. Assuming the instrument is not ready (i.e., is holding RXRDY LOW) the 96LS488 holds $\overline{\text{NRFD}}$ LOW preventing another data transfer from starting
g. Within $(t_{cp} + t_{PLH})$ of RXRDY going HIGH, $\overline{\text{NRFD}}$ goes HIGH and the next data transfer cycle can start

Fig. 8 Timing Diagram, Data Transfer from Bus to Listener


(a)
(b)

Data Transfer from Talker to GPIB (See *Figure 9*)

a. $\overline{\text{ATN}}$ goes HIGH after completion of a Talk address sequence; $\overline{\text{TAD}}$ (not shown) is already LOW.

b. Within (t_{cp} + t_{PHL}) $\overline{\text{DRB}}$ goes LOW to enable the bus drivers

c. At a time determined by the instrument logic, TXRDY goes HIGH

d. If $\overline{\text{NRFD}}$ is already HIGH, the 96LS488 drives $\overline{\text{DAV}}$ LOW after delay T1 (11 × t_{cp} + t_{PHL} in high or 20 × t_{cp} + t_{PHL} in low speed). If $\overline{\text{NRFD}}$ is LOW, $\overline{\text{DAV}}$ will stay HIGH until $\overline{\text{NRFD}}$ goes HIGH (assuming T1 has expired). The $\overline{\text{DAV}}$ LOW period corresponds to the Source Transfer State (STRS).

e. The Listener(s) respond by eventually taking $\overline{\text{NDAC}}$ HIGH

f. Within (t_{cp} + t_{PLH}) 96LS488 takes $\overline{\text{DAV}}$ HIGH and TXST HIGH to inform the instrument that the data has been accepted and a new byte can be presented.

g. The instrument takes TXRDY LOW and holds it there until it has provided a new byte, h or h'. The minimum time TXRDY must be LOW is t_{PWL}

h. If TXRDY pulses LOW within t_{cp} of TXST, TXST(H) will be a minimum of t_{cp} wide. Otherwise TXST goes LOW within (t_{cp} + t_{PHL}) of TXRDY,j. After the first byte is sent, T1 drops from 11 × t_{cp} to 5 × t_{cp} in high speed mode.

i. If TXRDY is HIGH before $\overline{\text{NRFD}}$, $\overline{\text{DAV}}$ goes LOW within T2 of $\overline{\text{NRFD}}$ going HIGH (5 × t_{cp} in high speed or 20 × t_{cp} in low speed)

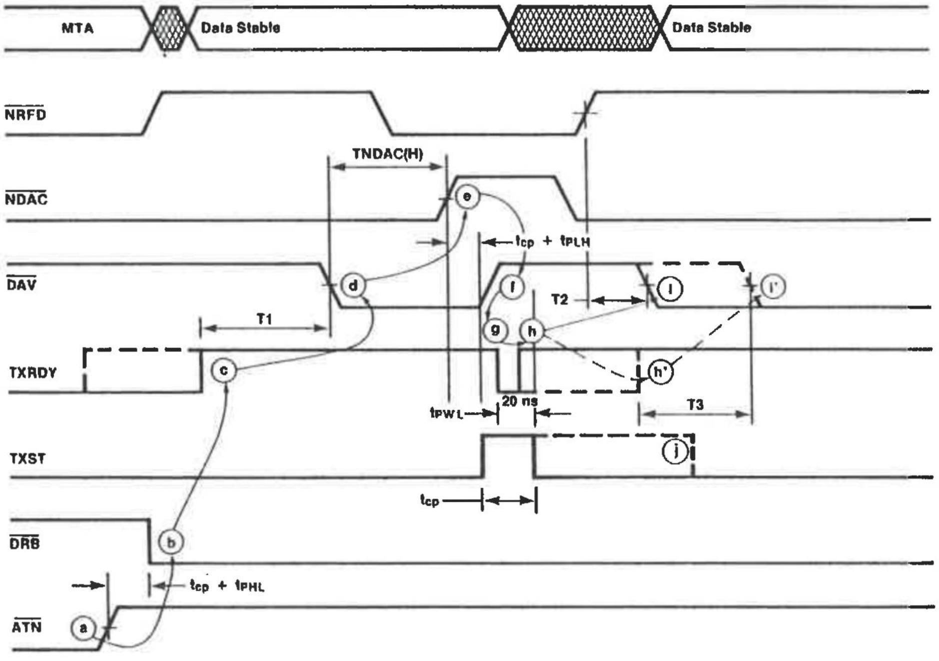
If TXRDY does not go HIGH until h' (after $\overline{\text{NRFD}}$ goes HIGH) $\overline{\text{DAV}}$ goes LOW T3 later,i'. (T3 = 6 × t_{cp} in HIGH and 21 × t_{cp} in low speed).

If the Talk sequence is interrupted by $\overline{\text{ATN}}$, while the instrument is generating a new byte, (between f and h), $\overline{\text{DRB}}$ will go HIGH within 200 ns and the $\overline{\text{DAV}}$ line will be relinquished. $\overline{\text{DRB}}$ will return LOW and the sequence will continue within (t_{cp} + t_{PLH}) of $\overline{\text{ATN}}$ going HIGH. If the 96LS488 is in high speed mode the first data byte sent will have a delay T1 = 11 × t_{cp}.

Note

In order to get the source handshake delays specified in IEEE Stad 488 - 1978, t_{cp} must be 100 ns (f_{clock} = 10 MHz).

Fig. 9 Timing Diagram Data Transfer from Talker to Bus



Notes

$\overline{\text{NRFD}}$, $\overline{\text{NDAC}}$ are driven by the current listener(s) $\overline{\text{DAV}}$ is driven by 96LS488.

T1 = 11 × t_{cp} + t_{PHL} in high speed, 20 × t_{cp} + t_{PHL} in low speed

T2 = 5 × t_{cp} + t_{PHL} in high speed, 20 × t_{cp} + t_{PHL} in low speed

T3 = 6 × t_{cp} + t_{PHL} in high speed, 21 × t_{cp} + t_{PHL} in low speed

Talk Address Sequence (See *Figure 10*)
This is similar to the Listen address sequence.

Fig. 10 Talk Address Sequence

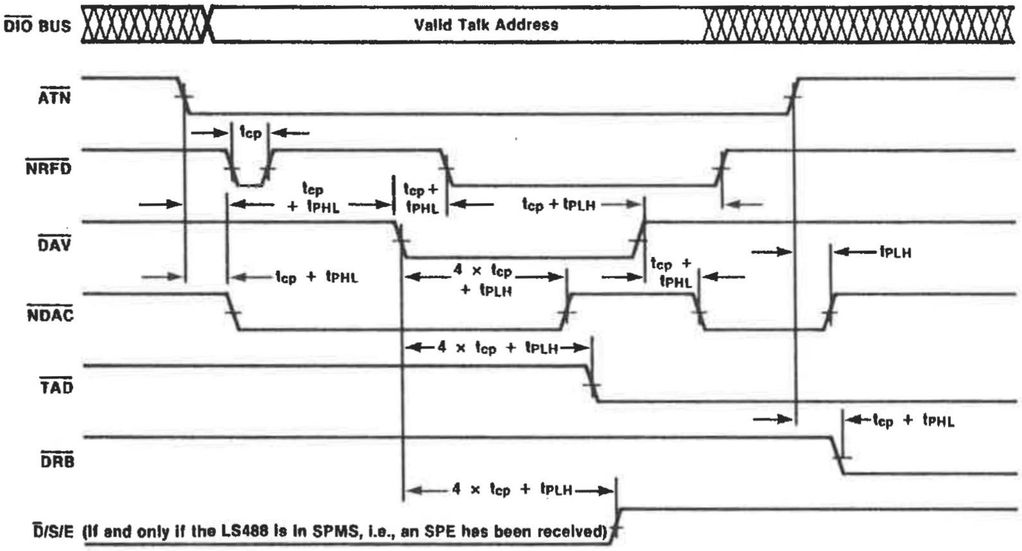

DIO BUS
Valid Talk Address
ATN
NRFD
DAV
NDAC
TAD
DRB
D/S/E (If and only if the LS488 is in SPMS, i.e., an SPE has been received)
tcp
tcp + tPHL
tcp + tPHL
tcp + tPLH
4 × tcp + tPLH
tcp + tPHL
tPLH
4 × tcp + tPLH
tcp + tPHL
4 × tcp + tPLH

Fig. 11 Timing Diagram for Secondary Address Sequence

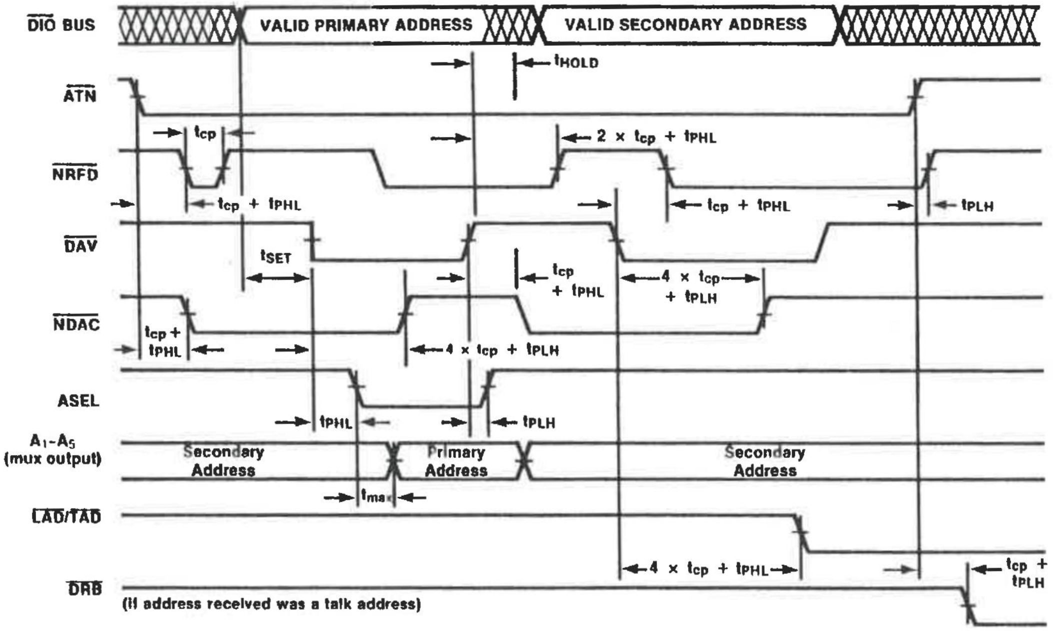
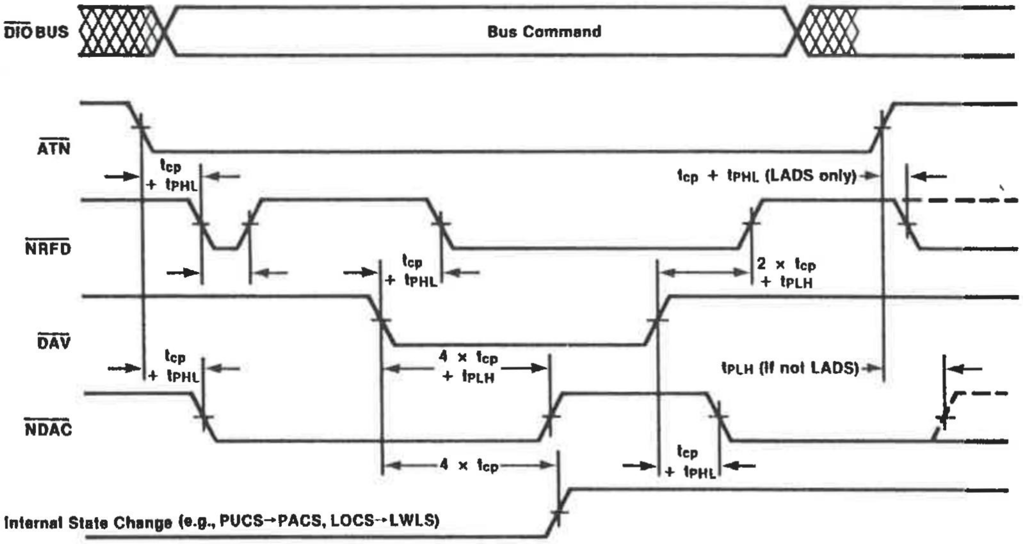

DIO BUS
VALID PRIMARY ADDRESS
VALID SECONDARY ADDRESS
ATN
tHOLD
NRFD
tcp
2 × tcp + tPHL
tcp + tPHL
tcp + tPHL
tPLH
DAV
tSET
tcp + tPHL
4 × tcp + tPLH
NDAC
tcp + tPHL
4 × tcp + tPLH
ASEL
tPHL
tPLH
A1-A5 (mux output)
Secondary Address
Primary Address
Secondary Address
tmax
LAD/TAD
4 × tcp + tPHL
tcp + tPLH
DRB
(If address received was a talk address)

Fig. 12 Timing Diagram for 96LS488 Receiving Bus Commands


DIO BUS
Bus Command
ATN
NRFD
DAV
NDAC
tcp + tPHL
tcp + tPHL (LADS only)
2 × tcp + tPLH
4 × tcp + tPLH
tPLH (If not LADS)
4 × tcp
Internal State Change (e.g., PUCS→PACS, LOCS→LWLS)

Note
Internal state changes do not necessarily change any 96LS488 outputs.

Fig. 13 Timing Diagram for Device Clear and Device Trigger Commands

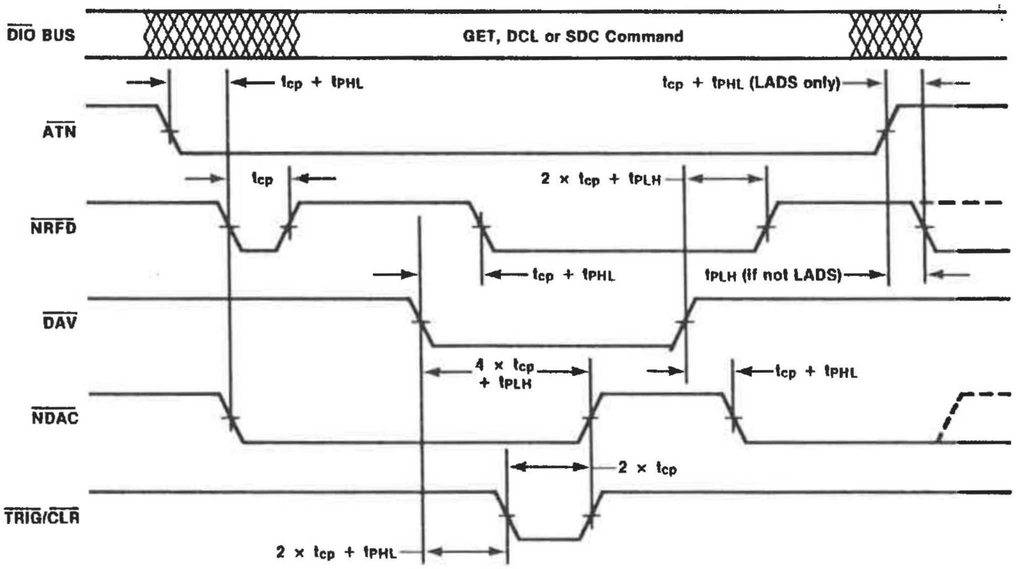
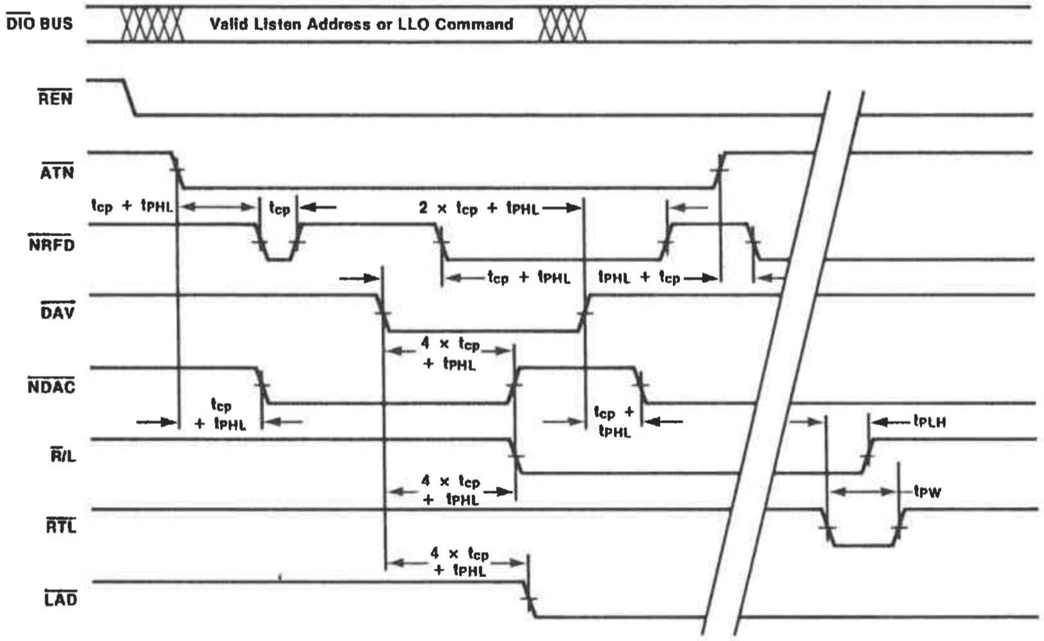
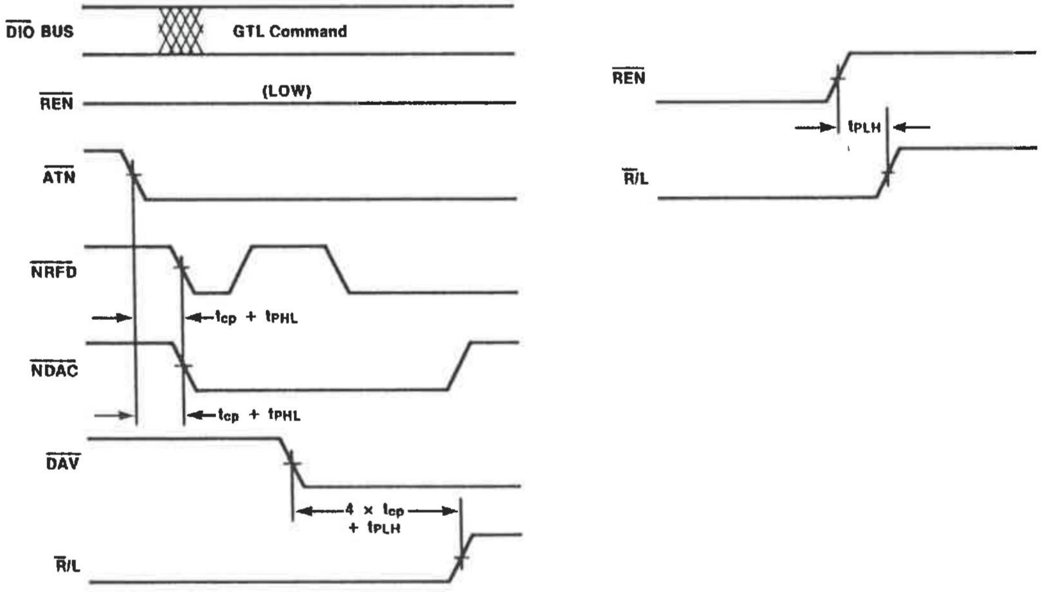

DIO BUS
GET, DCL or SDC Command
ATN
NRFD
DAV
NDAC
TRIG/CLR
tcp + tPHL
tcp + tPHL (LADS only)
tcp
2 × tcp + tPLH
tPLH (If not LADS)
4 × tcp + tPLH
2 × tcp
2 × tcp + tPHL

Fig. 14 Timing Diagram for Remote/Local Logic (Starting in LOCAL State)


DIO BUS
Valid Listen Address or LLO Command
REN
ATN
NRFD
DAV
NDAC
R/L
RTL
LAD
tcp + tPHL
tcp
2 × tcp + tPHL
tcp + tPHL
tPHL + tcp
4 × tcp + tPHL
tcp + tPHL
tcp + tPHL
tPLH
4 × tcp + tPHL
tPW
4 × tcp + tPHL

Note
If LLO has been sent, $\overline{\text{RTL}}$ will not cause $\overline{\text{R}}$/L to change.

Fig. 15 Timing Diagram for Remote/Local Logic (Starting in REMOTE State)


DIO BUS
GTL Command
REN
(LOW)
ATN
NRFD
tcp + tPHL
NDAC
tcp + tPHL
DAV
4 × tcp + tPLH
R/L
REN
tPLH
R/L

Serial Poll Sequence (See *Figure 16*)

a. The Controller has sent the Unlisten (UNL) and Serial Poll Enable (SPE) commands, generally in response to a LOW signal on $\overline{SRQ}$, and places a Talk address on the GPIB. The 96LS488 is sending the Service Requst ($\overline{SRQ}$) message, which was caused by the instrument logic making $\overline{RSV}$ LOW.

b. The 96LS488 allows $\overline{NRFD}$ to float passive HIGH to initiate normal handshake routine.

c. The Controller forces $\overline{DAV}$ LOW. Since $\overline{ATN}$ is also LOW, the 96LS488 receives the GPIB information as the message My Talk Address (MTA)

d. $\overline{NRFD}$ is active, acknowledging that the device is receiving a data byte

e. The 96LS488 enters the Talker Addressed State at time ($4 \times t_{cp} + t_{PHL}$) after $\overline{DAV}$ was forced LOW

f. $\overline{D}$/S/E goes HIGH at time ($4 \times t_{cp} + t_{PLH}$) after $\overline{DAV}$ was forced LOW. This indicates that the 96LS488 is in the Serial Poll Mode.

g. $\overline{NDAC}$ is allowed to float passive HIGH, indicating that the command data byte has been received

h. The Controller takes $\overline{DAV}$ HIGH

i. $\overline{NDAC}$ is pulled LOW, showing that the 96LS488 is ready for a new handshake cycle

j. The Controller allows the bus to float

k. The Controller releases $\overline{ATN}$. Because the 96LS488 is in the Serial Poll Mode, it now enters the Serial Poll Active State (SPAS), which prevails until the Controller makes $\overline{ATN}$ LOW again.

l. $\overline{DRB}$ goes active LOW, allowing the instrument to place its status byte on the bus. $\overline{DRB}$ goes LOW at time ($t_{cp} + t_{PHL}$) after $\overline{ATN}$ goes HIGH

m. When the 96LS488 enters SPAS, $\overline{SRQ}$ goes HIGH at time t_{PLH} after $\overline{ATN}$ goes HIGH

n. The instrument indicates that a status byte is ready by taking STRDY HIGH. This may occur earlier than shown, without affecting any of the foregoing

o. $\overline{DRB}$ enables the 3-state output $\overline{RQS}$ when in SPAS. $\overline{RQS}$ goes LOW at time ($t_{cp} + t_{PZL}$) after $\overline{ATN}$ is released

p. The Controller has taken $\overline{NRFD}$ HIGH, acknowledging that it is ready for the status byte

q. The 96LS488 takes $\overline{DAV}$ LOW after the time interval T_1, which starts either at the rising edge of STRDY or the falling edge of $\overline{DRB}$, whichever occurs later. The $\overline{DAV}$ LOW period corresponds to the Source Transfer State (STRS).

r. The Controller takes $\overline{NRFD}$ LOW

s. The instrument may release $\overline{RSV}$ at any time after the 96LS488 enters SPAS

t. The Controller takes $\overline{NDAC}$ HIGH, acknowledging that it has received the status byte

u. The 96LS488 releases $\overline{DAV}$ at time ($t_{cp} + t_{PLH}$) after $\overline{NDAC}$ goes HIGH

v. STST goes HIGH at time ($t_{cp} + t_{PLH}$) after $\overline{NDAC}$ goes HIGH. This tells the instrument that the status byte has been accepted. The instrument takes STRDY LOW to indicate that the data is no longer valid and to allow STST to go LOW again one t_{cp} after STRDY goes LOW

w. The Controller takes $\overline{NDAC}$ LOW once more after $\overline{DAV}$ goes HIGH

x. The data on the bus is no longer valid. If the $\overline{ATN}$ line remains HIGH, the instrument can provide another status byte by making STRDY HIGH to indicate valid data and to start the handshake

y. At the completion of the Serial Poll of this instrument, the Controller assumes control of the bus by forcing $\overline{ATN}$ LOW

z. $\overline{DRB}$ goes HIGH at time t_{PLH} after $\overline{ATN}$ goes LOW. This places the bus drivers of this instrument in the high-impedance (3-state output) or off (open-collector outputs) state

aa. Since $\overline{DRB}$ is no longer valid, the $\overline{RQS}$ output reverts to its high-impedance state

bb. $\overline{NRFD}$ goes HIGH, indicating that devices are ready to receive a command from the bus

cc. The Controller forces $\overline{DAV}$ LOW to show that it has placed a control byte on the bus

dd. $\overline{NRFD}$ goes LOW to acknowledge $\overline{DAV}$

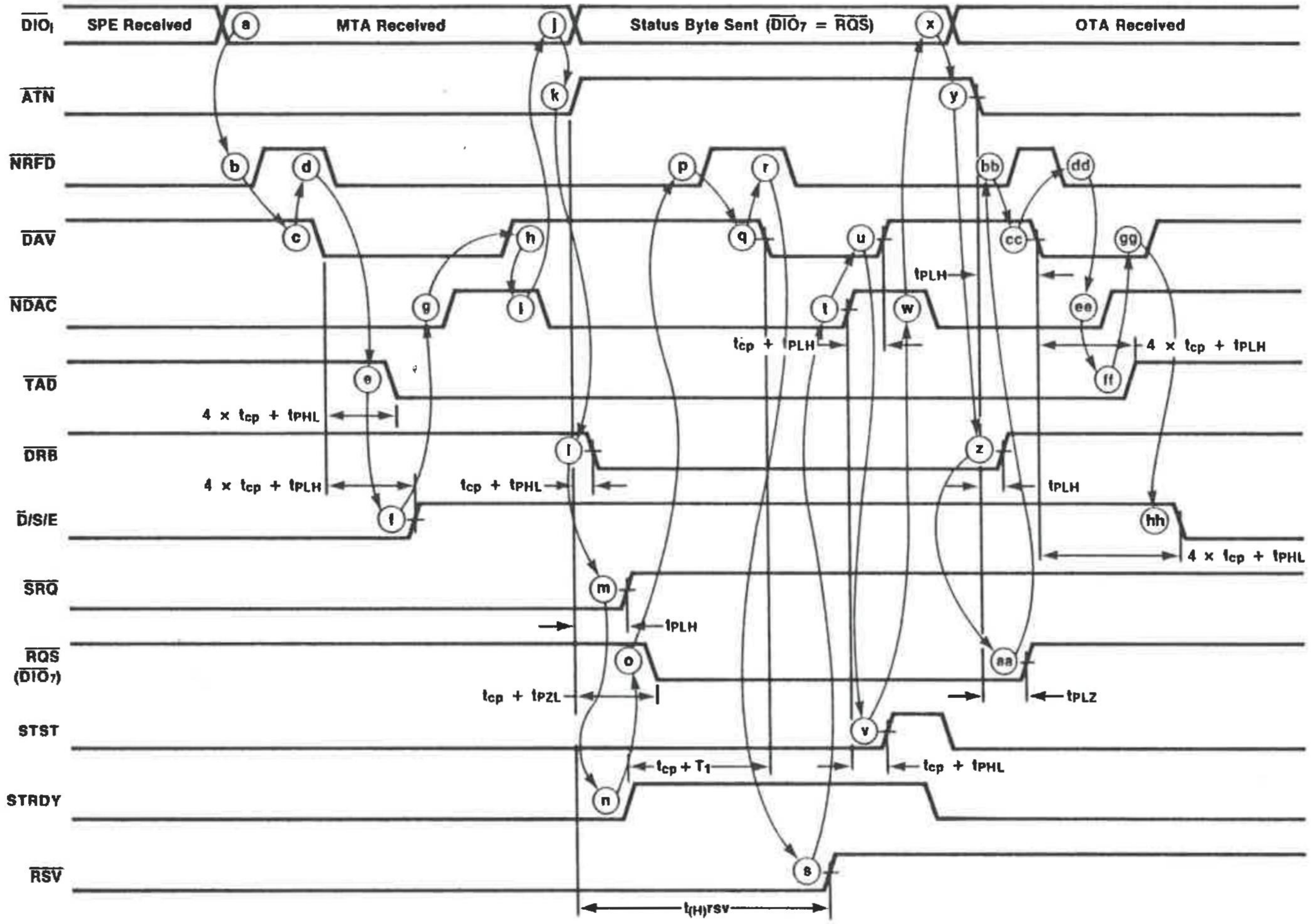
ee. $\overline{NDAC}$ goes HIGH when devices all acknowledge acceptance of the command byte

ff. The 96LS488 has received the Other Talk Address (OTA) command and reverts to its unaddressed state. $\overline{TAD}$ goes HIGH at time ($4 \times t_{cp} + t_{PLH}$) after $\overline{DAV}$ went LOW

gg. $\overline{DAV}$ is set HIGH by the Controller

hh. Because the 96LS488 has been unaddressed it is no longer in the Serial Poll Active State (SPAS). The $\overline{D}$/S/E output goes LOW at time ($4 \times t_{cp} + t_{PHL}$) after $\overline{DAV}$ went HIGH. The 96LS488 is still in the Serial Poll Mode State (SPMS), however, and will return to SPAS ($\overline{D}$/S/E HIGH, STST and STRDY valid) if subsequently addressed to talk. The 96LS488 enters the Serial Poll Idle State (SPIS) when the Controller either issues the Serial Poll Disable (SPD) command or makes $\overline{IFC}$ LOW.

Fig. 16 Timing Diagram for Serial Poll Sequence



$\overline{DIO}_i$
SPE Received
MTA Received
Status Byte Sent ($\overline{DIO}_7$ = $\overline{RQS}$)
OTA Received
$\overline{ATN}$
$\overline{NRFD}$
$\overline{DAV}$
$\overline{NDAC}$
$\overline{TAD}$
$\overline{DRB}$
$\overline{D}$/S/E
$\overline{SRQ}$
$\overline{RQS}$ ($\overline{DIO}_7$)
STST
STRDY
$\overline{RSV}$
a
b
c
d
e
f
g
h
i
j
k
l
m
n
o
p
q
r
s
t
u
v
w
x
y
z
aa
bb
cc
dd
ee
ff
gg
hh
4 × t_{cp} + t_{PHL}
4 × t_{cp} + t_{PLH}
t_{cp} + t_{PHL}
t_{PLH}
t_{cp} + t_{PZL}
t_{cp} + T_1
t_{cp} + t_{PLH}
t_{PLH}
t_{cp} + t_{PHL}
t_{PLH}
t_{PLZ}
4 × t_{cp} + t_{PLH}
4 × t_{cp} + t_{PHL}
$t_{(H)rsv}$

Parallel Poll Sequence (See *Figure 17*)

a. The Controller sends the instrument's listen address

b. Then Controller issues the Parallel Poll Configure command: this enables the 96LS488 to receive a subsequent PPE command.

c. The Controller issues the Parallel Poll Enable command. Bits $\overline{D}_1$–$\overline{D}_3$ of the command byte determine which data output ($\overline{DIO}_j$) will be valid when the IDY command is sent. Bit $\overline{D}_4$ of the command is compared with IST (Instrument Status) during the IDY command.

d. The Controller issues the Unlisten command. The 96LS488 will now not respond to further PPE commands, allowing the Controller to configure other instruments.

e. The Instrument Status bit (IST) is set by the instrument before an IDENTIFY command is received. IST must be in a stable state when IDY is received so the setup and hold times must be observed (t_s IST and t_h IST).

f. During the IDY command the Controller releases the data lines $\overline{DIO}_1$–$\overline{DIO}_7$, $\overline{DO}_8$. The assigned data line $\overline{DIO}_j$ will be taken active LOW by the 96LS488 if IST compares with bit $\overline{D}_4$ of the PPE command.

g. The IDY message is received (IDY = $\overline{EOI}$ • $\overline{ATN}$). At this time the Instrument Status bit IST is latched in the 96LS488, and the output data $\overline{DIO}_j$ is true if IST compares with bit $\overline{D}_4$ of the PPE command. $\overline{DIO}_j$ is LOW if $\overline{D}_4$ was LOW and IST was HIGH, or if $\overline{D}_4$ was HIGH and IST was LOW.

h. The 96LS488 enables data bit $\overline{DIO}_j$ after a delay t_{PHL} from the time $\overline{EOI}$ goes active LOW. $\overline{DIO}_j$ remains valid while IDY is active. Note that this is an asynchronous message sent and is not governed by the handshake protocol.

i. IST may be altered not less than time t_h IST after IDY is active. Because IST is latched by IDY it will not affect the status byte sent during this IDY routine.

j. IDY is false and the 96LS488 stops sending a status byte. Outputs $\overline{DIO}_1$-$\overline{DIO}_7$, $\overline{DO}_8$ again float passive HIGH.

k. The status bit $\overline{DIO}_j$ floats passive HIGH at a time not greater than t_{PLH} after IDY goes FALSE.

l. The Controller can now place information on the data bus.

m. Once the 96LS488 has been configured via steps a-c, the Controller can examine IST at any time by issuing the IDY command. To change the $\overline{D}_1$-$\overline{D}_4$ assignment of a particular 96LS488, the Controller must address it to listen, issue the PPC command, then the Parallel Poll Disable (PPD) command (which clears the $\overline{D}_1$-$\overline{D}_4$ latches), then the PPE command with the revised $\overline{D}_1$-$\overline{D}_4$ assignment. The $\overline{D}_1$-$\overline{D}_4$ assignment will also be cleared by the universal Parallel Poll Unconfigure (PPU) command or by $\overline{MR}$, but not by $\overline{IFC}$. PPU, $\overline{MR}$ or the MLA/PPC/PPD sequence puts the 96LS488 in the Parallel Poll Idle State (PPIS) and it will not respond to IDY until it is subsequently reconfigured.

Fig. 17 Timing Diagram for Parallel Poll Sequence

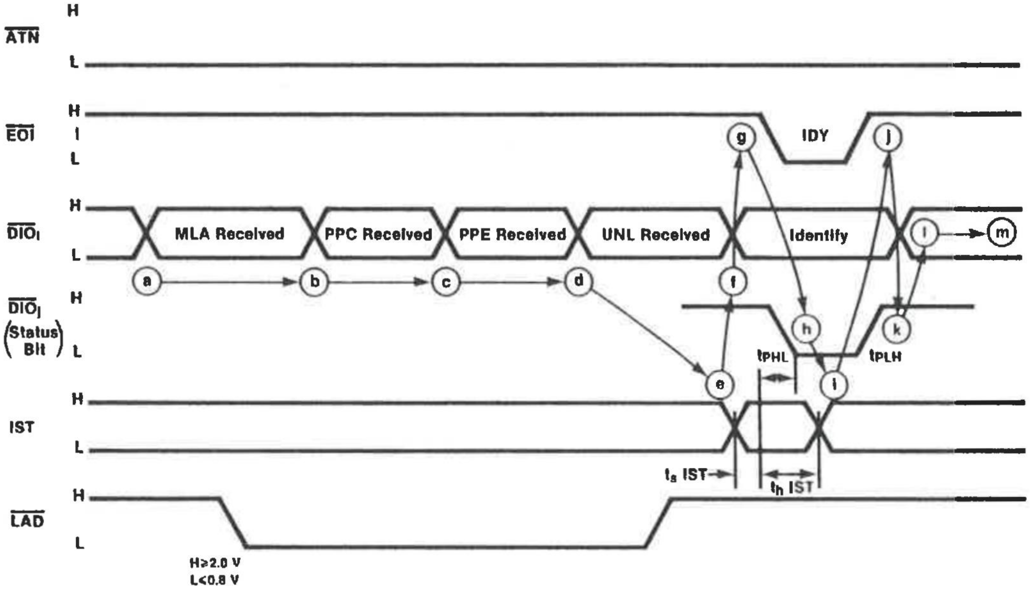
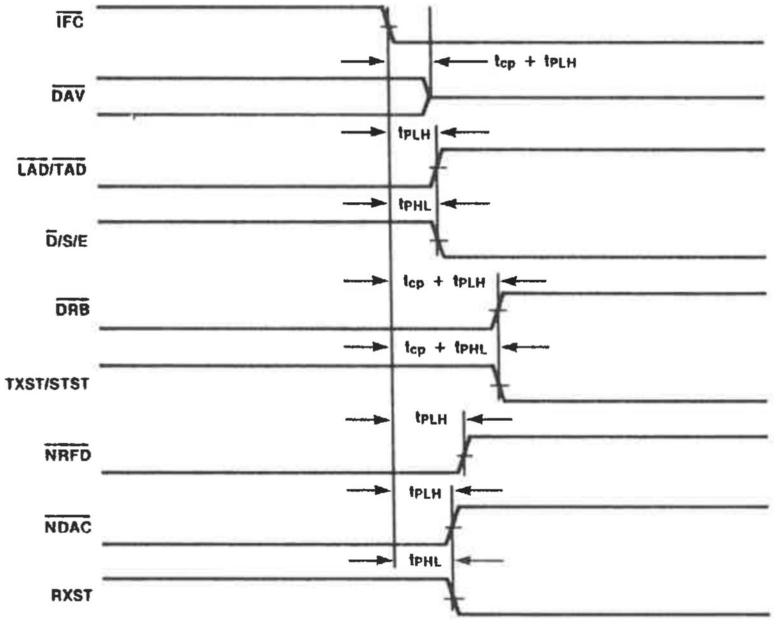


Fig. 18 IFC Timing Diagram


IFC
DAV
LAD/TAD
D/S/E
DRB
TXST/STST
NRFD
NDAC
RXST
tcp + tPLH
tPLH
tPHL
tcp + tPLH
tcp + tPHL
tPLH
tPLH
tPHL

Absolute Maximum Ratings
(above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

DC Characteristics

Symbol	Parameter	Min	Max	Unit	V_{CC}	Condition
V_{IH}	Input HIGH Voltage All Inputs	2.0		V		Recognized as a HIGH Signal Over Recommended V_{CC} and T_A Range
V_{IL}	Input LOW Voltage DM All Inputs DC		0.7 0.8	V		Recognized as a LOW Signal Over Recommended V_{CC} and T_A Range
V_{T+}-V_{T-}	Hysteresis Voltage	0.4		V		All Bus Inputs
V_{CD}	Input Clamp Diode Voltage		1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage $\overline{\text{RQS}}$, $\overline{\text{DAV}}$	2.5		V	Min	I_{OH} = −5.2 mA
	$\overline{\text{DIO}}_1$ − $\overline{\text{DIO}}_7$, $\overline{\text{DO}}_8$, $\overline{\text{SRQ}}$, $\overline{\text{NRFD}}$, $\overline{\text{NDAC}}$	2.5	3.7	V	Min	Open-Collector Bus Pins I_{OH} = 0 mA
	$\overline{\text{R}}$/L, $\overline{\text{D}}$/S/E, RXST, TXST, STST, $\overline{\text{CLR}}$, $\overline{\text{TRIG}}$, $\overline{\text{DRB}}$, ASEL, XTAL, $\overline{\text{LAD}}$, $\overline{\text{TAD}}$	2.5		V	Min	I_{OH} = −0.4 mA
V_{OL}	Output LOW Voltage $\overline{\text{DIO}}_1$ − $\overline{\text{DIO}}_7$, $\overline{\text{DO}}_8$, $\overline{\text{SRQ}}$, $\overline{\text{RQS}}$, $\overline{\text{NRFD}}$, $\overline{\text{NDAC}}$, $\overline{\text{DAV}}$		0.5	V	Min	I_{OL} = 48 mA
	All Other Outputs DM, DC		0.4	V	Min	I_{OL} = 4.0 mA
	DC		0.5	V	Min	I_{OL} = 8.0 mA
I_{IH}	0.5 U.L. Input HIGH Current 1.0 U.L. n U.L.		20 40 n(40)	µA	Max	I_{IH} = 40 µA Multiplied by Input HIGH U.L. Shown on Data Sheet; V_{IN} = 2.7 V
I_{IL}	0.25 U.L. Input LOW Current 0.5 U.L. n U.L.		−0.4 −0.8 n(−1.6)	mA	Max	I_{IL} = −1.6 mA Multiplied by Input LOW U.L. Shown on Data Sheet; V_{IN} = 0.4 V
I_{POFS}	Leakage into GPIB Pins in Powered-off State		100	µA	0	V_{IN} = 2.5 V
I_{OZH}	3-State Output OFF Current HIGH		40	µA	Max	V_{OUT} = 2.4 V
I_{OZL}	3-State Output OFF Current LOW		−40	µA	Max	V_{OUT} = 0.4 V
I_{CC}	Power Supply Current	*	250	mA	Max	Any 3 Bus Outputs in LOW State

*Typical Value for I_{CC} is 180 mA.

AC Characteristics V_{CC} = 5.0 V, T_A = +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Fig. No.	Condition
f_{max}	Maximum Clock Frequency	12	15		MHz		For correct timing for SH or AH, $\overline{CP}$ must be 10 MHz.
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to $\overline{NRFD}$		150 90		ns ns	7, 8, 10, 11 12, 13, 14	C_L = 300 pF, R_L = 200 Ω
t_{PLH}	Propagation Delay $\overline{ATN}$ to $\overline{NRFD}$		150		ns	11	C_L = 300 pF, R_L = 200 Ω
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to $\overline{NDAC}$		150 90		ns ns	7, 8, 10, 11 12, 13, 14	C_L = 300 pF, R_L = 200 Ω
t_{PLH}	Propagation Delay $\overline{ATN}$ to $\overline{NDAC}$		150		ns	10, 12, 13	C_L = 300 pF, R_L = 200 Ω
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to $\overline{DAV}$		100 90		ns ns	9	C_L = 300 pF, R_L = 200 Ω
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{ATN}$ to $\overline{DAV}$		100 100		ns ns	9	C_L = 300 pF, R_L = 200 Ω
t_{PZL} t_{PZH}	Output Enable Time $\overline{CP}$ to $\overline{DAV}$		100 100		ns ns	9	C_L = 300 pF, R_L = 200 Ω
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{CP}$ to $\overline{DAV}$		100 100		ns ns		C_L = 300 pF, R_L = 200 Ω
t_{PLH}	Propagation Delay $\overline{IFC}$ to $\overline{NRFD}$ or $\overline{NDAC}$		180		ns	18	C_L = 300 pF, R_L = 200 Ω
t_{PHL}	Propagation Delay $\overline{IFC}$ to RXST		160		ns	18	C_L = 15 pF
t_{PHL}	Propagation Delay, $\overline{IFC}$ to $\overline{D}$/S/E		100		ns	18	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to $\overline{LAD}$ or $\overline{TAD}$		150 150		ns ns	7, 8, 10	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay $M_0 - M_3$ to $\overline{LAD}$ or $\overline{TAD}$		60 60		ns ns		C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to RXST, TXST or STST		75 75		ns ns	8, 9	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to $\overline{DRB}$		85 85		ns ns	9, 11	C_L = 15 pF
$t_{\ LH}$	Propagation Delay, $\overline{ATN}$ to $\overline{DRB}$		70		ns	9	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to $\overline{TRIG}$ or $\overline{CLR}$		130 130		ns ns	13	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{DAV}$ to ASEL		25 25		ns ns	11	C_L = 15 pF

AC Characteristics $V_{CC} = 5.0\text{ V}$, $T_A = +25°\text{C}$ (Cont'd)

Symbol	Parameter	Min	Typ	Max	Unit	Fig. No.	Condition
t_{PHL}	Propagation Delay, $\overline{\text{MR}}$ to RXST, TXST, STST, $\overline{\text{D}}$/S/E		100		ns		$C_L = 15\text{ pF}$
t_{PLH}	Propagation Delay $\overline{\text{MR}}$ to $\overline{\text{LAD}}$, $\overline{\text{TAD}}$ or $\overline{\text{R}}$/L		50		ns		$C_L = 15\text{ pF}$
t_{PLH}	Propagation Delay, $\overline{\text{MR}}$ to $\overline{\text{NRFD}}$, $\overline{\text{NDAC}}$, $\overline{\text{DAV}}$, $\overline{\text{DIO}_1}$-$\overline{\text{DIO}_7}$, $\overline{\text{DO}_8}$ or $\overline{\text{SRQ}}$		100		ns		$C_L = 300\text{ pF}$, $R_L = 200\ \Omega$
t_{PLH} t_{PHL}	Propagation Delay $\overline{\text{CP}}$ to XTAL		15 15		ns ns	6	$C_L = 15\text{ pF}$, $\overline{\text{CP}}$ driven from ext. oscillator
t_{PLH} t_{PHL}	Propagation Delay, $\overline{\text{CP}}$ to $\overline{\text{R}}$/L		150 150		ns ns	14, 15	$C_L = 15\text{ pF}$
t_{PLH}	Propagation Delay, $\overline{\text{RTL}}$ to $\overline{\text{R}}$/L		150		ns	14	$C_L = 15\text{ pF}$
t_{PLH}	Propagation Delay, $\overline{\text{REN}}$ to $\overline{\text{R}}$/L		45		ns	14	$C_L = 15\text{ pF}$
t_{PLH} t_{PHL}	Propagation Delay, $\overline{\text{CP}}$ to $\overline{\text{D}}$/S/E		140 140		ns ns	16	$C_L = 15\text{ pF}$
t_{PLH} t_{PHL}	Propagation Delay, $\overline{\text{RSV}}$ to $\overline{\text{SRQ}}$		90 30		ns ns		$C_L = 300\text{ pF}$, $R_L = 200\ \Omega$
t_{PLH}	Propagation Delay, $\overline{\text{ATN}}$ to $\overline{\text{SRQ}}$		150		ns	16	$C_L = 300\text{ pF}$, $R_L = 200\ \Omega$
t_{PZL} t_{PZH}	Output Enable Time, $\overline{\text{CP}}$ to $\overline{\text{RQS}}$		100 100		ns ns	16	$C_L = 300\text{ pF}$, $R_L = 200\ \Omega$
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{\text{ATN}}$ to $\overline{\text{RQS}}$		85 85		ns ns	16	$C_L = 300\text{ pF}$, $R_L = 200\ \Omega$
t_{PLH} t_{PHL}	Propagation Delay $\overline{\text{EOI}}$ to $\overline{\text{DIO}_1}$-$\overline{\text{DIO}_7}$, $\overline{\text{DO}_8}$		110 50		ns ns	17	$C_L = 300\text{ pF}$, $R_L = 200\ \Omega$
t_{PLH} t_{PHL}	Propagation Delay $\overline{\text{EOI}}$ to $\overline{\text{D}}$/S/E		30 30		ns ns		$C_L = 15\text{ pF}$

AC Operating Requirements $V_{CC} = 5.0\ \mathrm{V}$, $T_A = +25\,°\mathrm{C}$

Symbol	Parameter	Min	Typ	Max	Unit	Fig. No.	Condition
t_s (L) t_s (H)	Setup Time, HIGH or LOW IST to $\overline{\mathrm{EOI}}$	20 20			ns ns	17	
t_h (L) t_h (H)	Hold Time, HIGH or LOW IST to $\overline{\mathrm{EOI}}$	5.0 5.0			ns ns	17	
t_s (L)	Setup Time, $\overline{\mathrm{RSV}}$ to $\overline{\mathrm{ATN}}$		−50		ns		Device about to enter SPAS on next L to H $\overline{\mathrm{ATN}}$ transition.
t_h (L)	Hold Time, $\overline{\mathrm{RSV}}$ to $\overline{\mathrm{ATN}}$		−50		ns		Device about to enter SPAS on next L to H $\overline{\mathrm{ATN}}$ transition.
t_s (H) t_s (L)	Setup Time, HIGH or LOW $\overline{\mathrm{DIO}}_1$–$\overline{\mathrm{DIO}}_7$ to $\overline{\mathrm{DAV}}$	100 100			ns ns	11	
t_h (H) t_h (L)	Hold Time, HIGH or LOW $\overline{\mathrm{DIO}}_1$–$\overline{\mathrm{DIO}}_7$ to $\overline{\mathrm{DAV}}$	0 0			ns ns	11	
t_m (H) t_m (L)	Delay in external address mux from ASEL to valid address			100 100	ns ns	11	
t_w (H) t_w (L)	$\overline{\mathrm{CP}}$ Pulse Width	30 30			ns ns		
t_w (L)	Pulse Width RXRDY, TXRDY or STRDY	20			ns	8, 9, 16	
t_w (L)	$\overline{\mathrm{MR}}$ Pulse Width	50			ns		
t_w (L)	$\overline{\mathrm{RTL}}$ Pulse Width	60			ns	14	

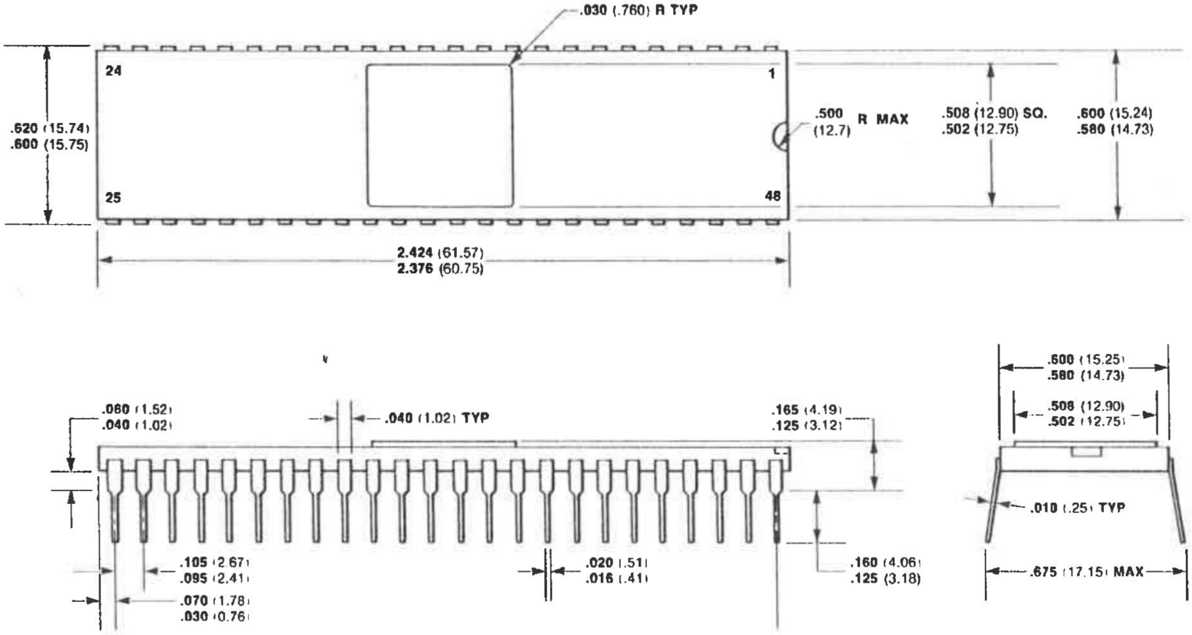
Ordering Information

Order Code	Package	Temperature*
96LS488DC	Ceramic DIP	Commercial
96LS488DM	Ceramic DIP	Military

*C = 0°C to +70°C
M = −55°C to +125°C

Package Outlines

48-Pin Side-brazed Package


.030 (.760) R TYP
24
1
25
48
.620 (15.74)
.600 (15.75)
.500 (12.7) R MAX
.508 (12.90) SQ.
.502 (12.75)
.600 (15.24)
.580 (14.73)
2.424 (61.57)
2.376 (60.75)
.060 (1.52)
.040 (1.02)
.040 (1.02) TYP
.165 (4.19)
.125 (3.12)
.105 (2.67)
.095 (2.41)
.070 (1.78)
.030 (0.76)
.020 (.51)
.016 (.41)
.160 (4.06)
.125 (3.18)
.600 (15.25)
.580 (14.73)
.508 (12.90)
.502 (12.75)
.010 (.25) TYP
.675 (17.15) MAX

Notes
All dimensions in inches **bold** and millimeters in parentheses
Pin material is nickel, gold-plated kovar or alloy 42
Cap is kovar or alloy 42
Base is ceramic
Cavity size is .310 × .310 (7.874 × 7.874)
Package weight is 7.7 grams

Fairchild cannot assume responsibility for use of any circuitry described other than circuitry embodied in a Fairchild product. No other circuit patent licenses are implied.

Manufactured under one of the following U.S. Patents: 2981877, 3015048, 3064167, 3108359, 3117260; other patents pending.